

CHELSEA DJ2 UMA Schematics Document

AMD Danube CPU S1G4

RS880M + SB820M

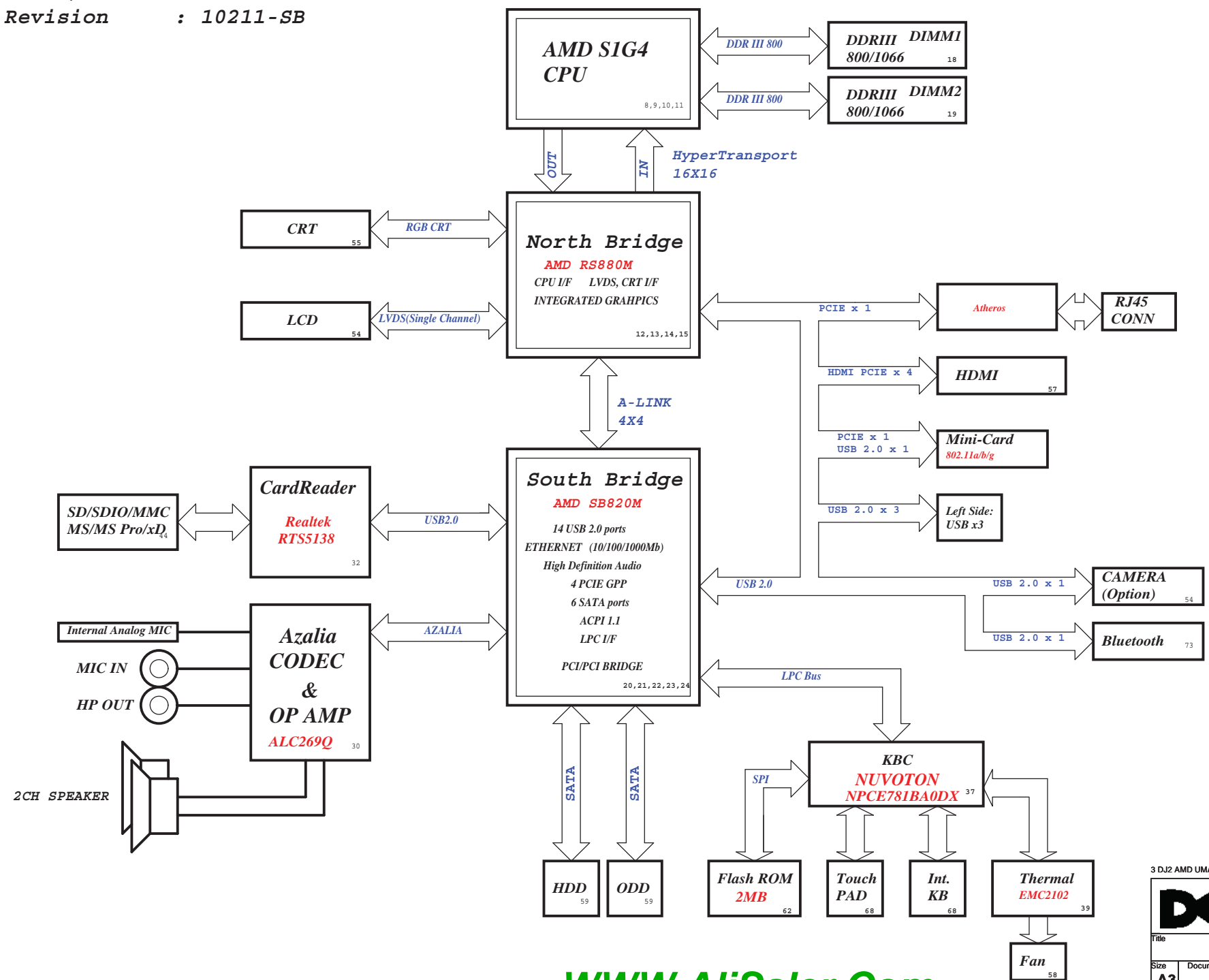
2010-04-13

REV : X01



Project code: 91.4EM01.001
PCB P/N : 48.4EM18.0SA
Revision : 10211-SB

Chelsea DJ2 AMD UMA Block Diagram



CHARGER	
BQ24745RHDR	
INPUTS	OUTPUTS
+DC_IN_SS +CHAGER_SRC	+PWR_SRC
SYSTEM DC/DC	
RT8205BGQW-GP 46	
INPUTS	OUTPUTS
+PWR_SRC	+5V_ALW2 +3.3V_RTC_LDO +5V_ALW +3.3V_ALW
SYSTEM DC/DC	
RT8209EGQW 50	
INPUTS	OUTPUTS
+PWR_SRC	+1.1V_RUN
CPU CORE	
ISL6265AHTZ-T-GP 47	
INPUTS	OUTPUTS
+PWR_SRC	+VCC_CORE +VDDNB
DDR III SUS&VTT	
TPS51116RGER 49	
INPUTS	OUTPUTS
+PWR_SRC	+1.5V_SUS
SYSTEM DC/DC	
APL5930KAI 52	
INPUTS	OUTPUTS
+3.3V_ALW	+1.8V_RUN
SYSTEM DC/DC	
Swithes/RT9013 42,53	
INPUTS	OUTPUTS
+3.3V_ALW +5V_ALW +1.5V_SUS +3.3V_RUN	+3.3V_RUN +5V_RUN +1.5V_RUN +2.5V_RUN
SYSTEM DC/DC	
TPS51125RGER 48,51	
INPUTS	OUTPUTS
+3.3V_ALW +1.5V_SUS	+1.1V_ALW +CPU_VDDR
PCB LAYER	
L1: Top L2: VCC L3: Signal L4: Signal L5: GND L6: Bottom	

3 DJ2 AMD UMA (10 100 w HDMI)

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title _____

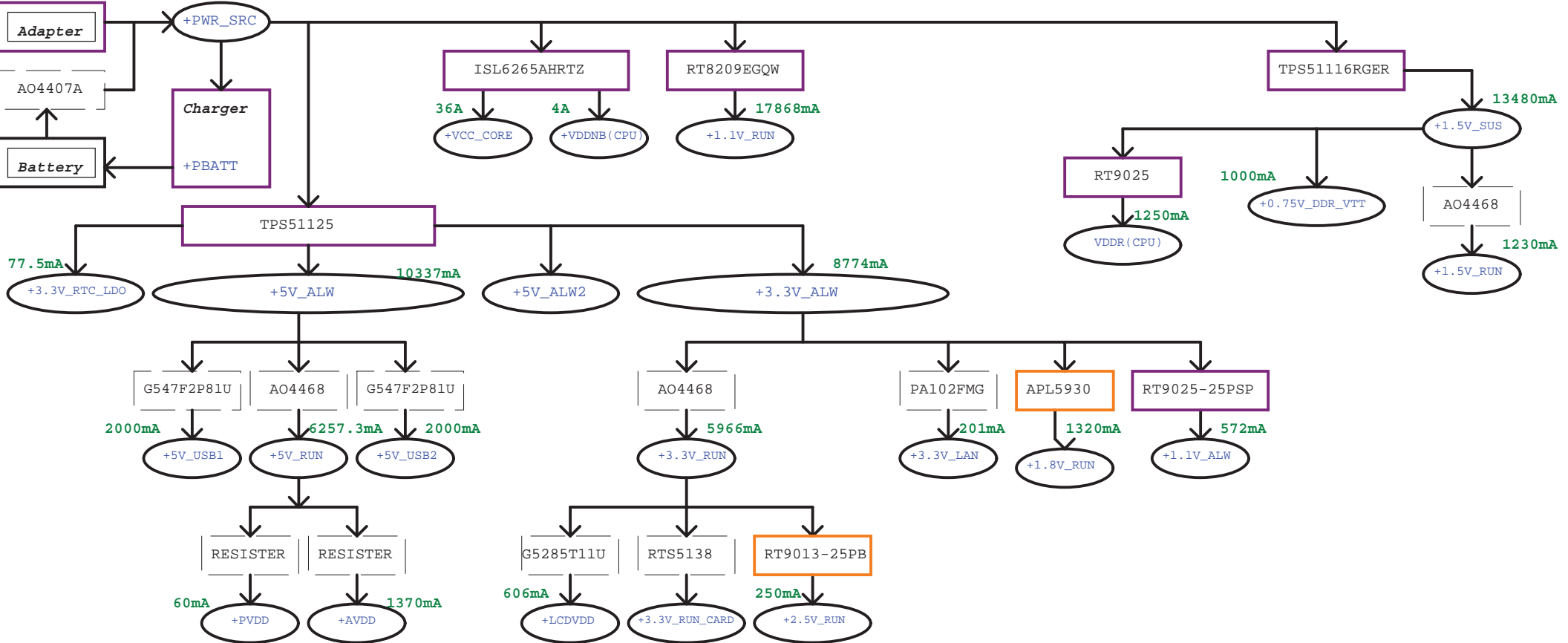
Block Diagram

Size	Document Number	Rev
A3	Chelsea DJ2 AMD UMA	X01

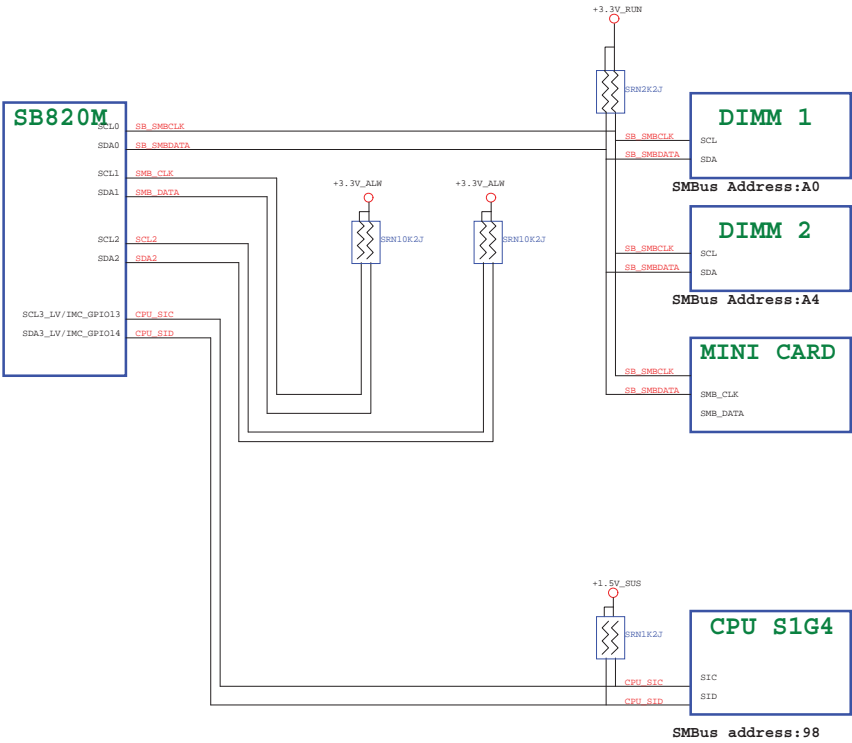
Date: Tuesday, April 13, 2010 Sheet 2 of 90

Power Block Diagram

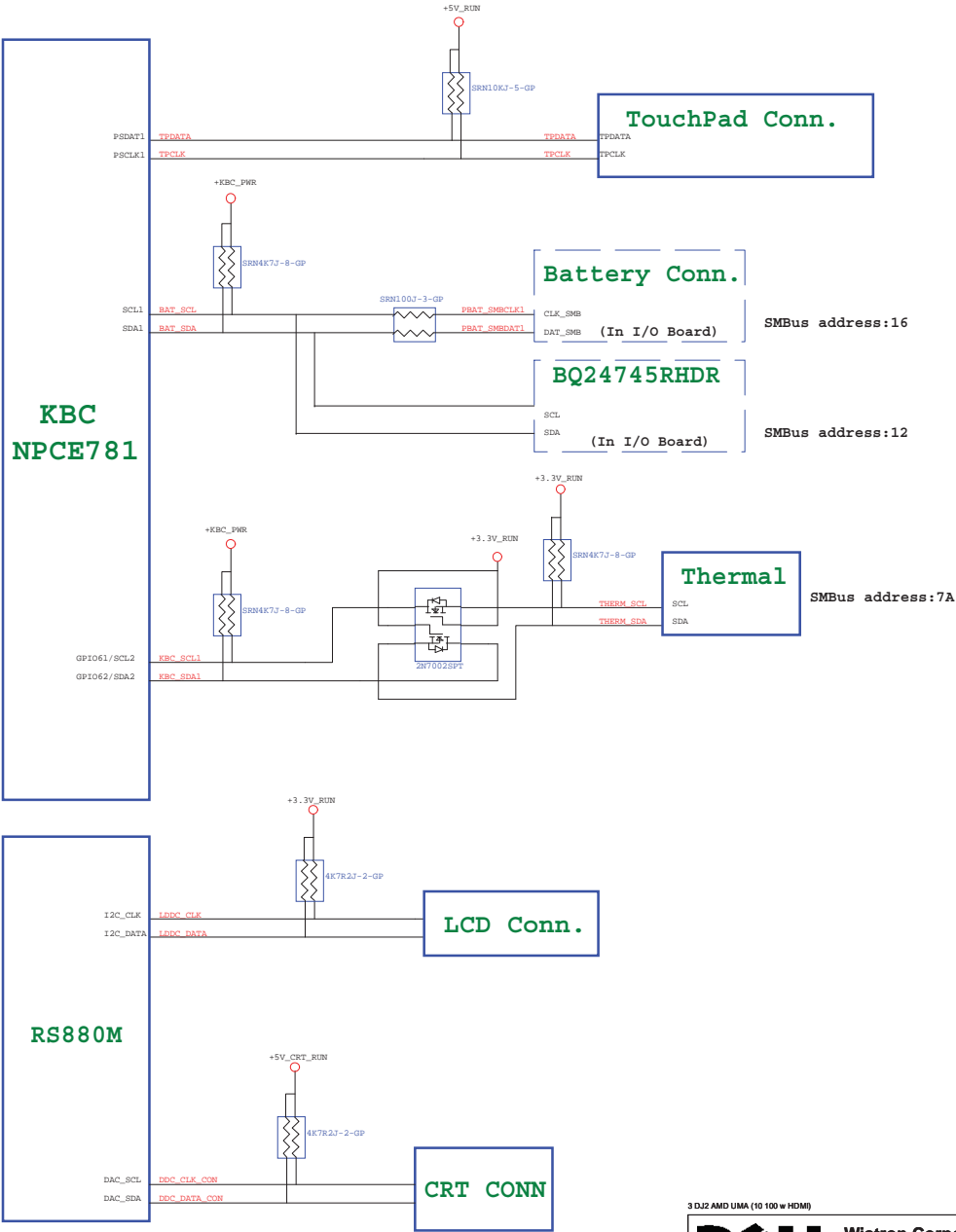
Power Shape



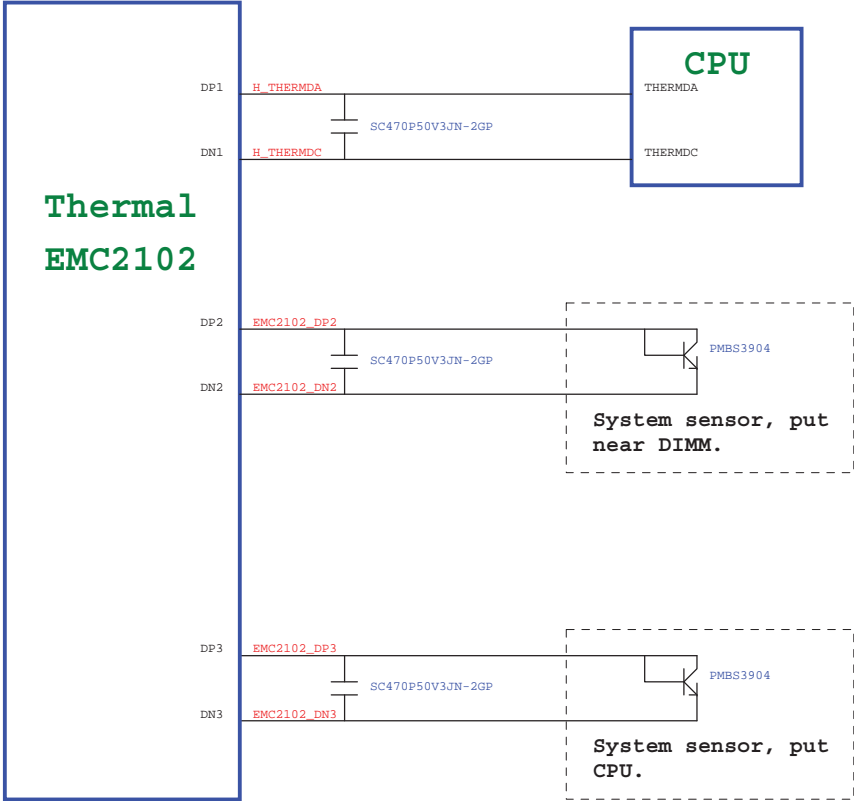
SB820M SMBus Block Diagram



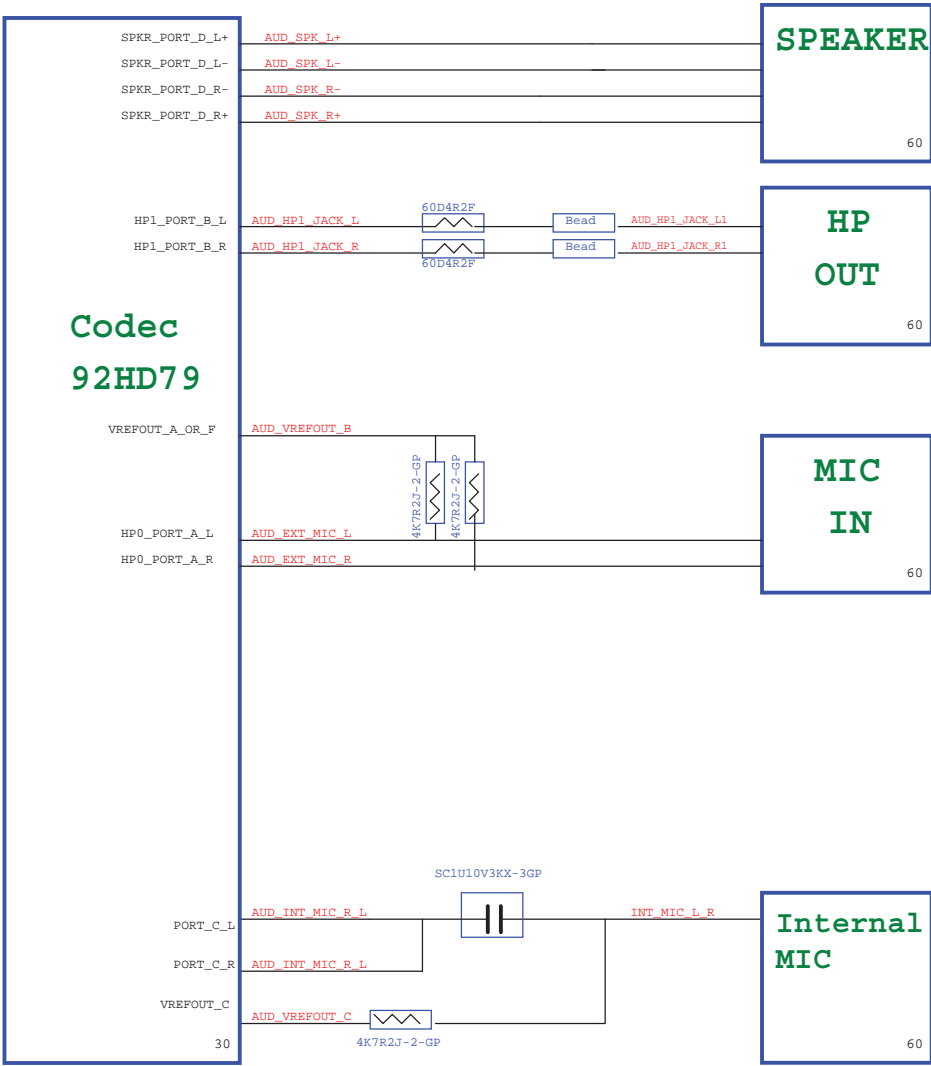
KBC SMBus Block Diagram



Thermal Block Diagram



Audio Block Diagram



NB880M Strapping

Capture from 46113 rs880m ds nda 1.03

Name	Strap Name	Schematic Note
LPCCLK0	ECEnableStrap	Embedded Controller (EC) * 0 V - Disabled 3.3 V - Enabled
EC_PWM3 EC_PWM2	{ROMTYPE_1, ROMTYPE_0 }	ROMTYPE_1 ROMTYPE_0 ROM TYPE 3.3V 0V SPI ROM 3.3V 3.3V Reserved 0V 0V Firmware Hub 0V 3.3V LPC ROM * (supports both LPC and PMC ROM types)
LPCCLK1	CLKGEN	Defines clock generator 0V - External clock mode: Use 100-MHz PCIeR clock as reference clock and generate i nternal clocks only. * 3.3V- Integrated clock mode: Use 25-MHz crystal clock and generate both internal and external clocks
PCICLK1	BIF_GEN2 COMPLIANCE_Strap	Set PCIe to Gen II mode 0V- Force PCIe interface at Gen I mode * 3.3V- PCIe interface is at Gen II mode Not Applicable to SB820M but provision for pull-down is required.
PCICLK2	BootFailTmrEn	Watchdog function * 0V- Disable the boot fail timer function 3.3V- Enable the boot fail timer function
PCICLK3	DefaultStrapMode	Default Debug Straps * 0V- Disable Debug Straps. 3.3V- Select external Debug Straps
PCICLK4	CPUClkSel	CPU/NB HT Clock Selection 0V- Reserved. * 3.3V- Required setting for integrated clock mode. This strap is not used if the strap CLKGEN is configured for external clock generator mode.
AZ_SDOUT	CoreSpeedMode	Slow down core clock for low power platform. * 0V- Performance mode 3.3V- Low Power mode

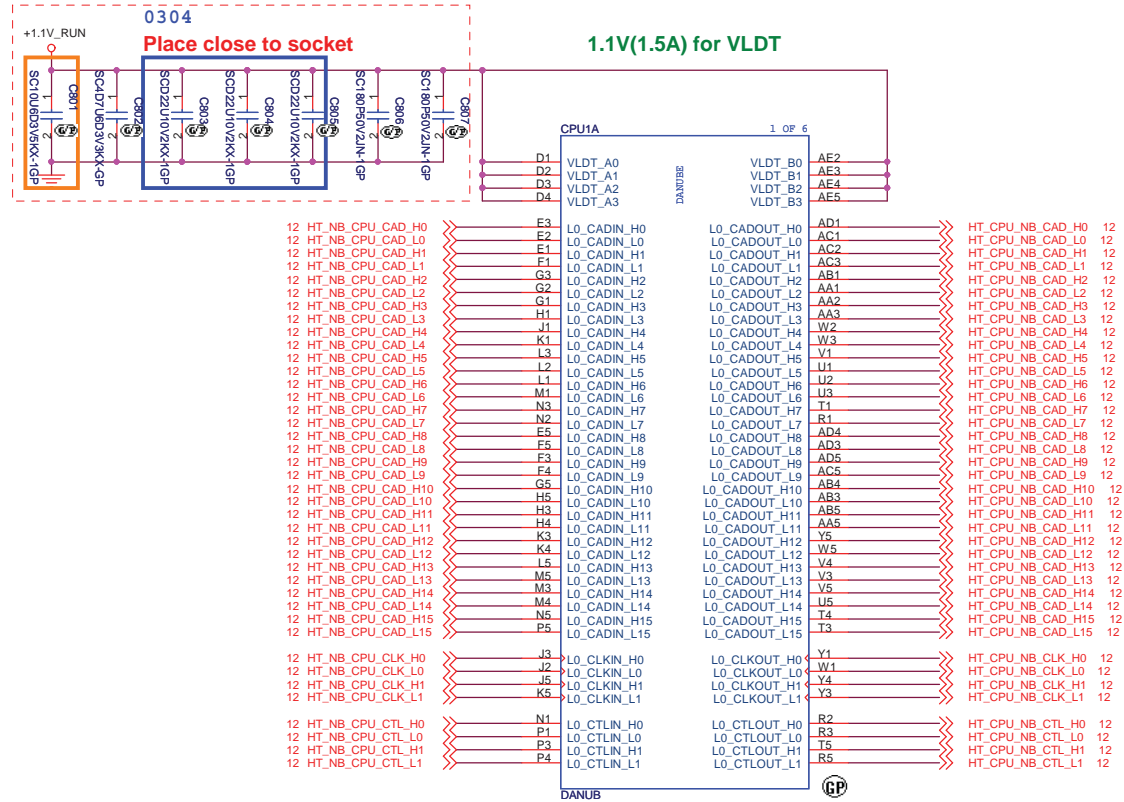
Name	Strap Function	Schematic Note
DAC_VSYNC	STRAP_DEBUG_BUS_GPIO _ENABLE#	Enables debug bus access through memory I/O pads and GPIOs. 0: Enable 1: Disable
DAC_HSYNC	SIDE_PORT_EN#	Indicates if memory side-port is available or not 0: Available 1: Not available
SUS_STAT#	LOAD_EEPROM_STRAPS#	Selects loading of strap values from EEPROM. 0: I2C master can load strap values from EEPROM if connected, or use default values if EEPROM is not connected. Please refer to RS880M's reference schematics for system level implementation details. 1: Use default values

USB Table

USB	
Pair	Device
0	USB1
1	USB3
2	USB2
3	USB1 (I/O Board, 17")
4	WLAN
5	Reserve
6	Reserve
7	Reserve
8	Reserve
9	Reserve
10	CARD READER
11	CAMERA
12	BLUETOOTH
13	Reserve

PCIe Routing

LANE0	MiniCard WLAN
LANE1	LAN



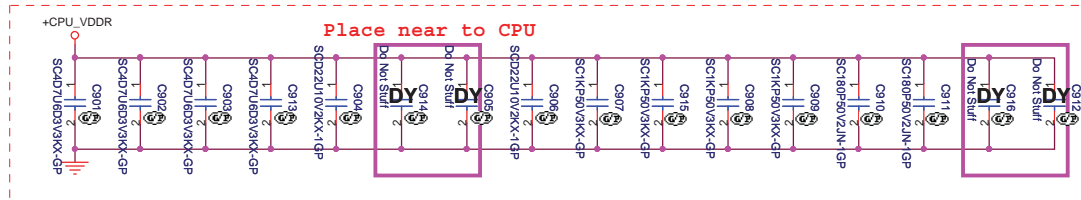
SKT-BGA638H176

1'nd 62.10055.111

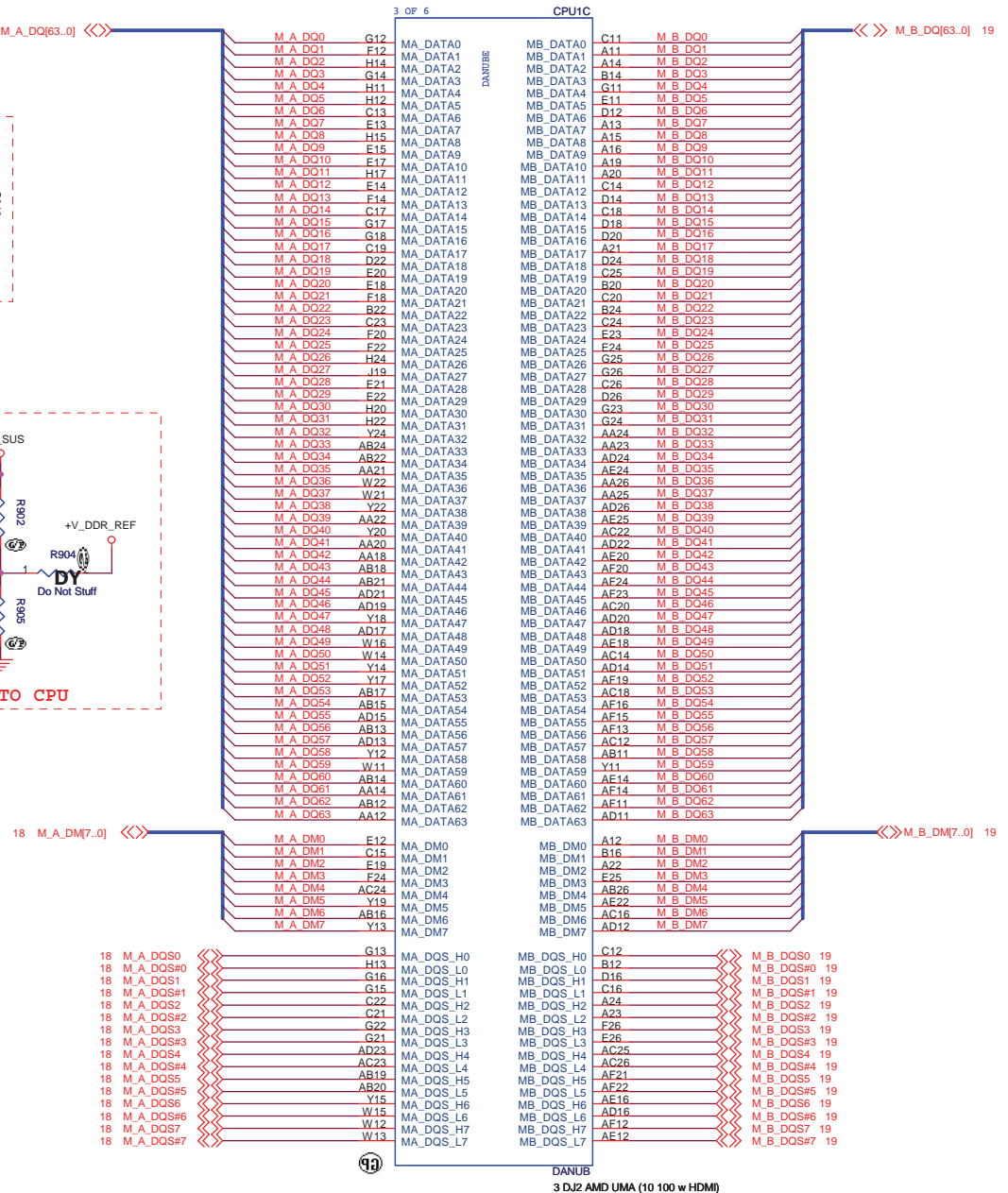
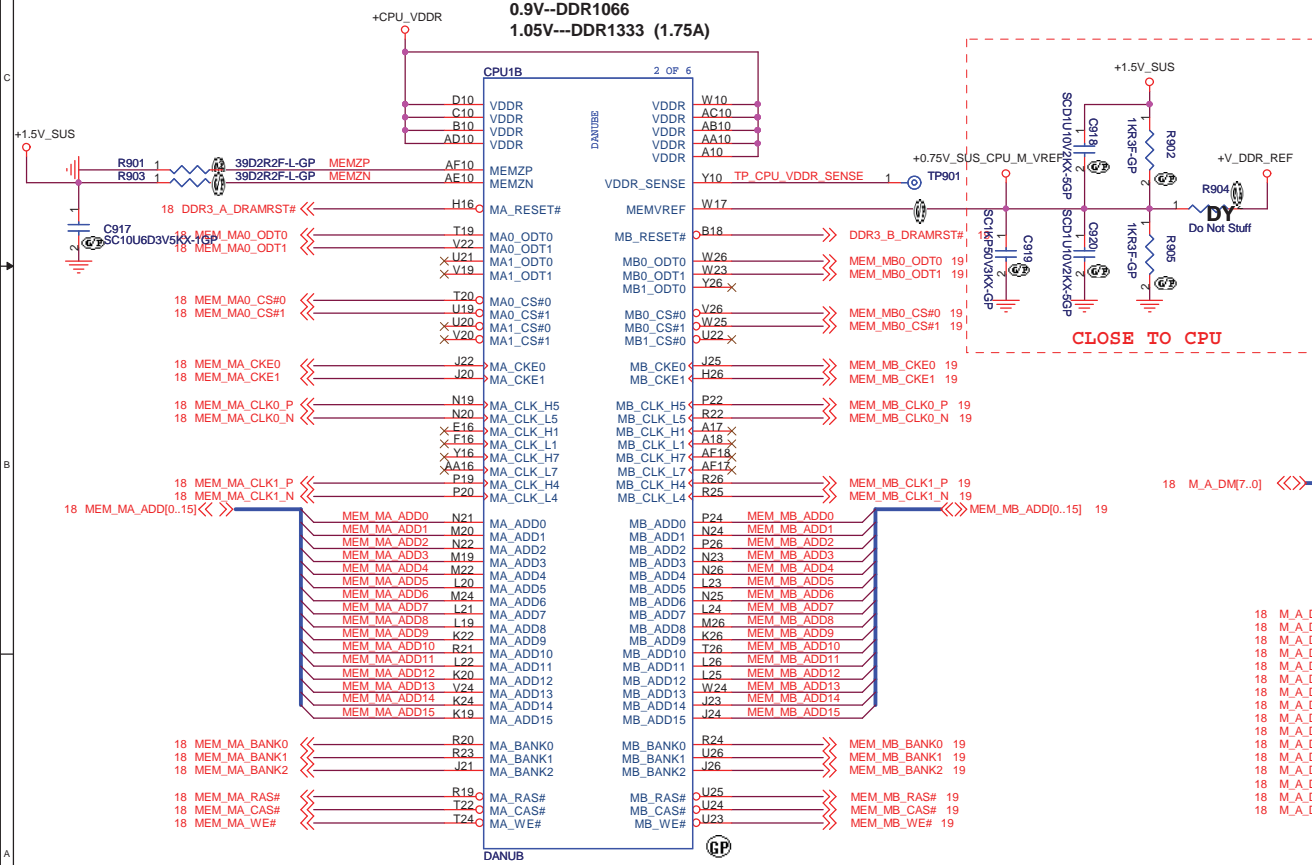
2'nd 62.10055.181

3 DJ2 AMD UMA (10 100 w HDMI)

DELL		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,		Taipei Hsien 221, Taiwan, R.O.C.	
Title CPU_HT_LINK I/F_(1/4)			
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0.9V(1.25A) for VDDR
0.9V--DDR1066
1.05V---DDR1333 (1.75A)

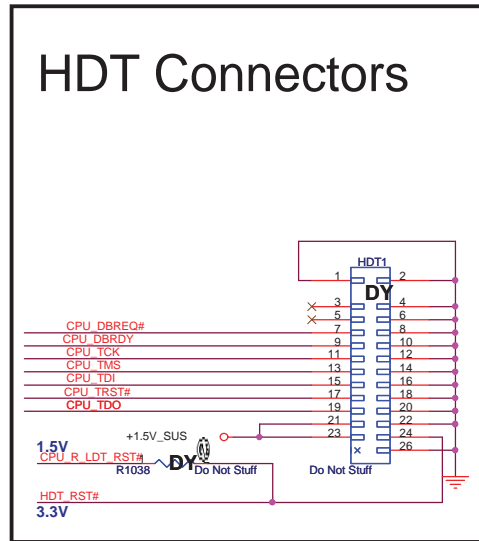


DANUB

3 DJ2 AMD UMA (10 100 w HDMI)



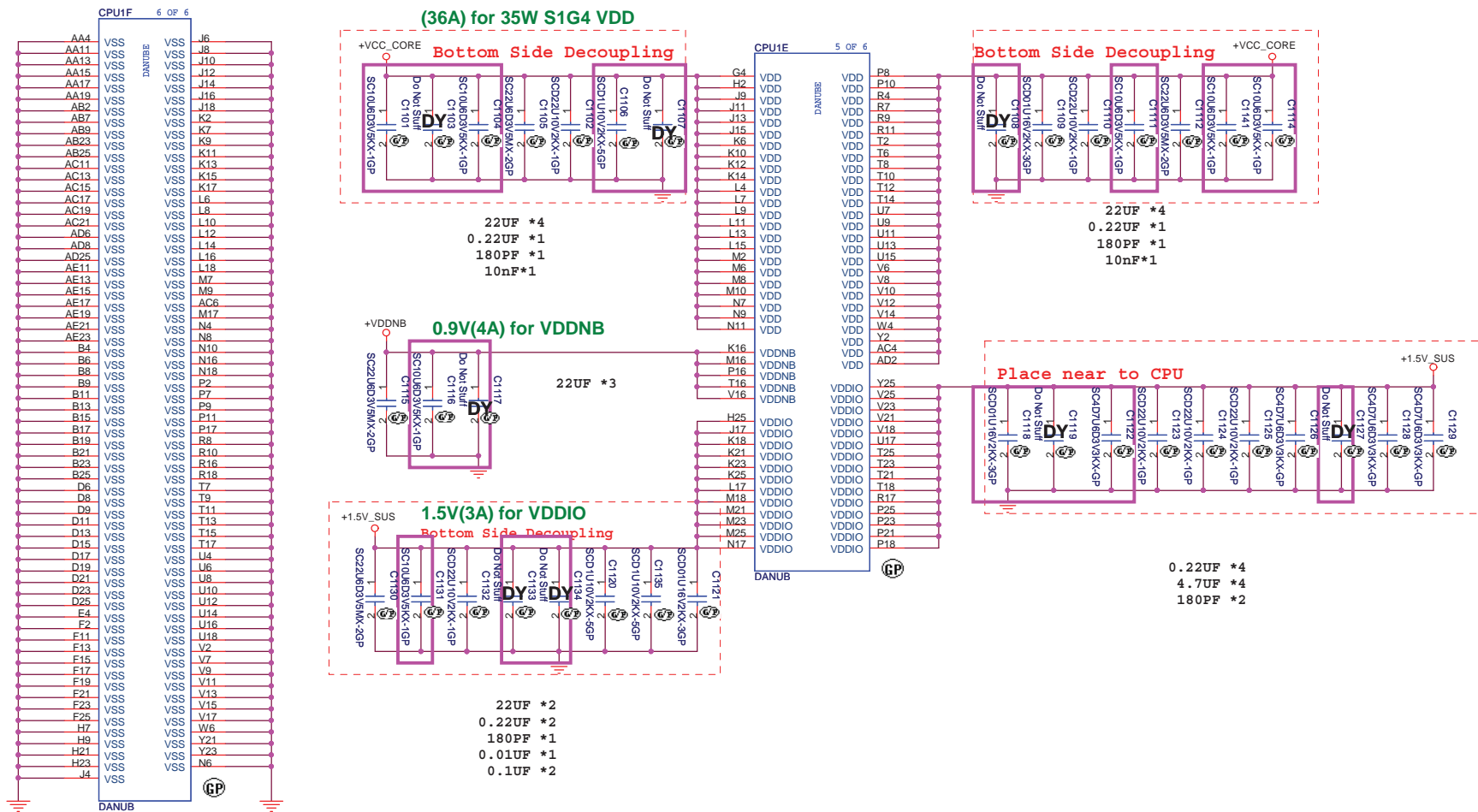
LYAOUT:ROUTE VDDA TRACE APPROX.
50mils WIDE(USE 2X25 mil TRACES TO
EXIT BALL FIELD),AND 500 mils LONG.



DELL **Wistron Corporation**
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3 DJ2 AMD UMA (10 100 w HDMI)

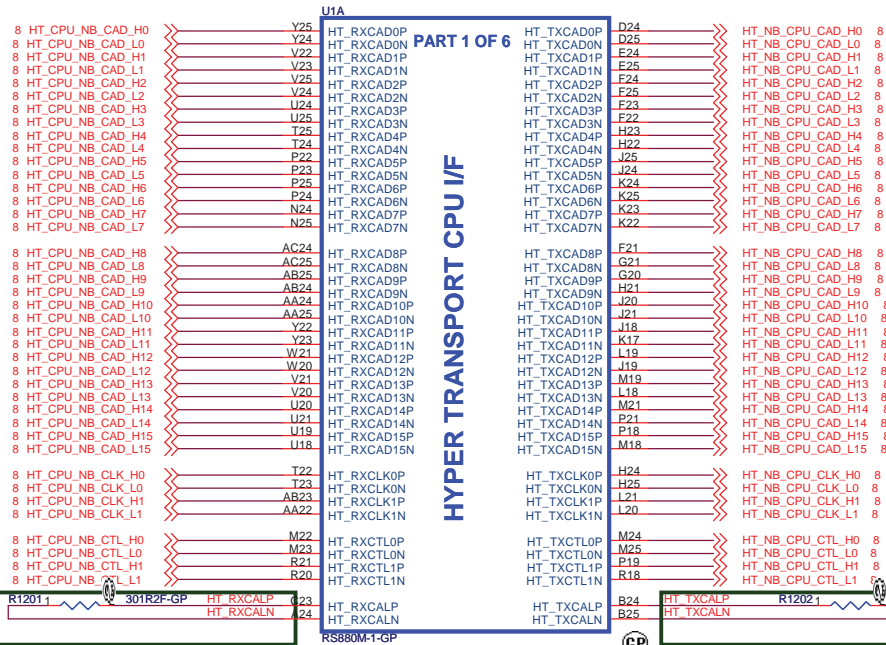


Title	CPU_Power_(4/4)
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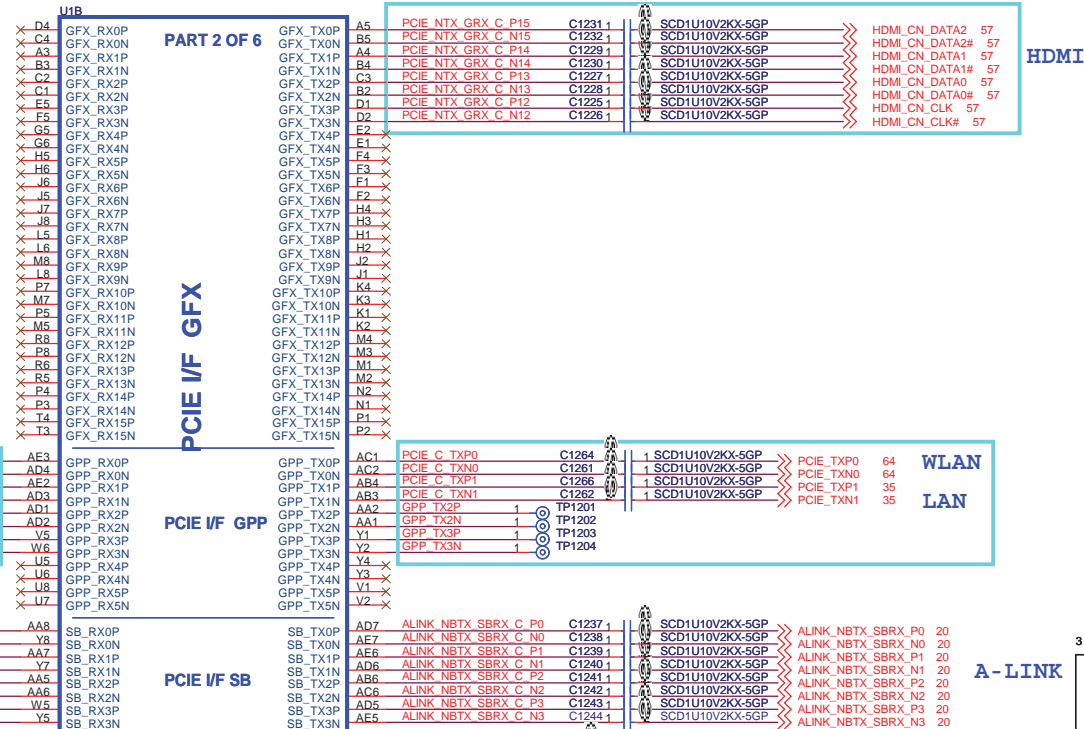
SSID = N.B

RS880M : 71.RS880.M05



```
Place < 1000mils from pin C23 and A2
```

Place < 1000mils from pin B25 and B24



A-LINK

A-LINK

RS880M-1-GP

Place: 10 miles from AC8 and AB8

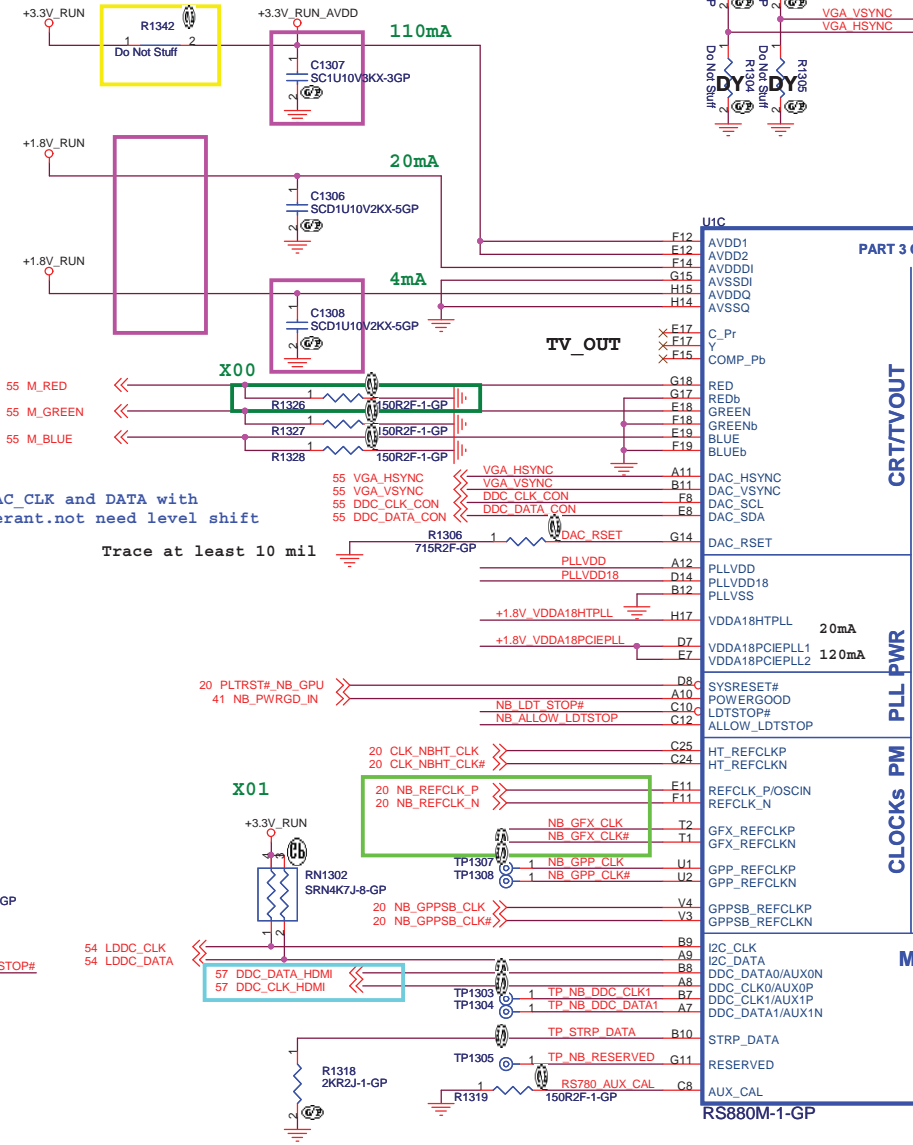
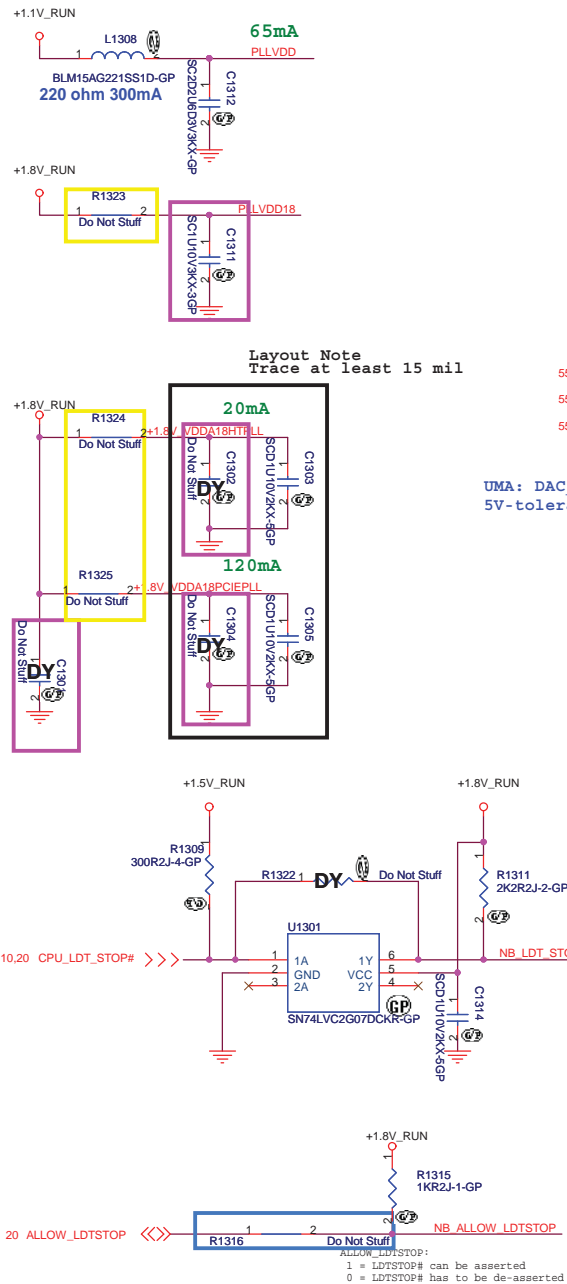
3 DJ2 AMD UMA (10 100 w HDMI)



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SSID = N.B

RS880M : 71.RS880.M05

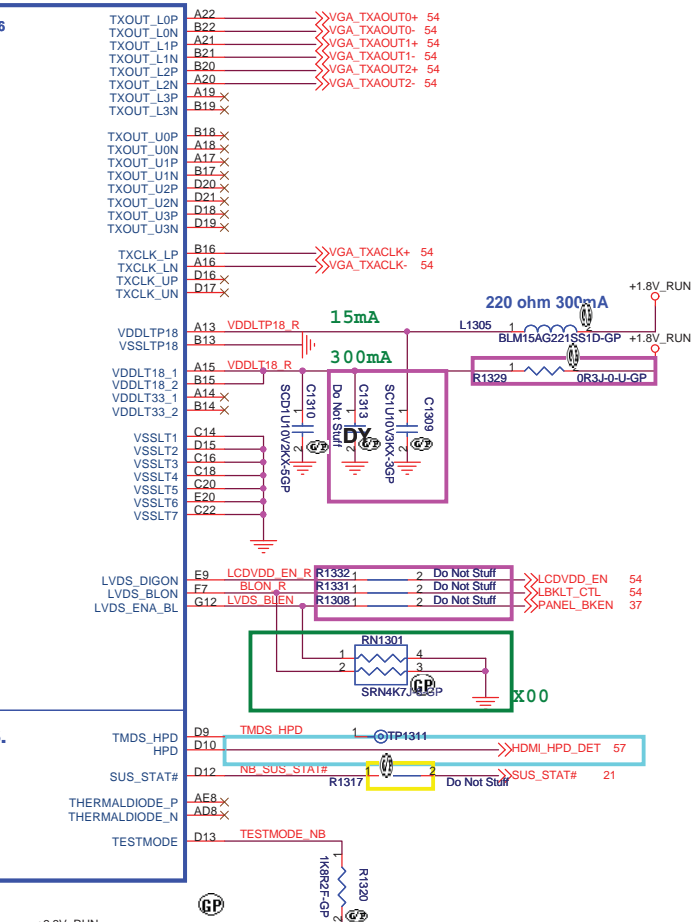


STRAP_DEBUG_BUS_GPIO_ENABLE# (RS880M use VGA_VSYN)
Enables debug bus access through memory I/O pads and GPIOs.
*1 : Disable
0 : Enable

SIDE_PORT_EN# (RS880M use VGA_HSYN)
*1 = Memory Side port Not available
0 = Memory Side port available

LOAD_EEPROM_STRAPS#(RS880M use SUS_STAT#)
Selects Loading of STRAPS From EEPROM
*1 : use Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

***DEFAULT**



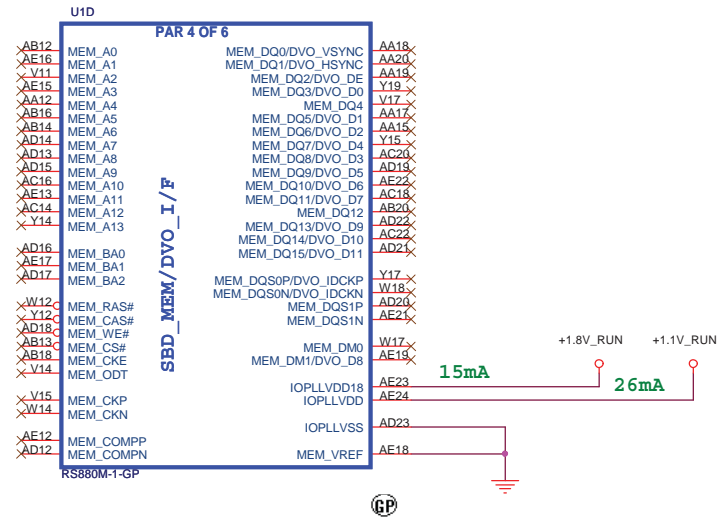
3 DJ2 AMD UMA (10 100 w HDMI)

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Taipei Hsien 221, Taiwan, R.O.C.

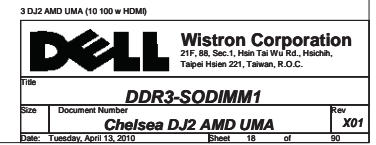
Title **AMD-RS880M_LVDS&CRT_(2/4)**

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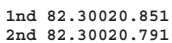




SB700 A12 : 71.SB800.M02

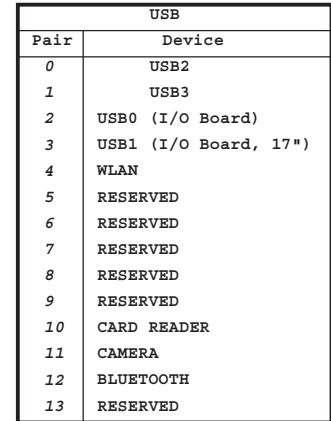


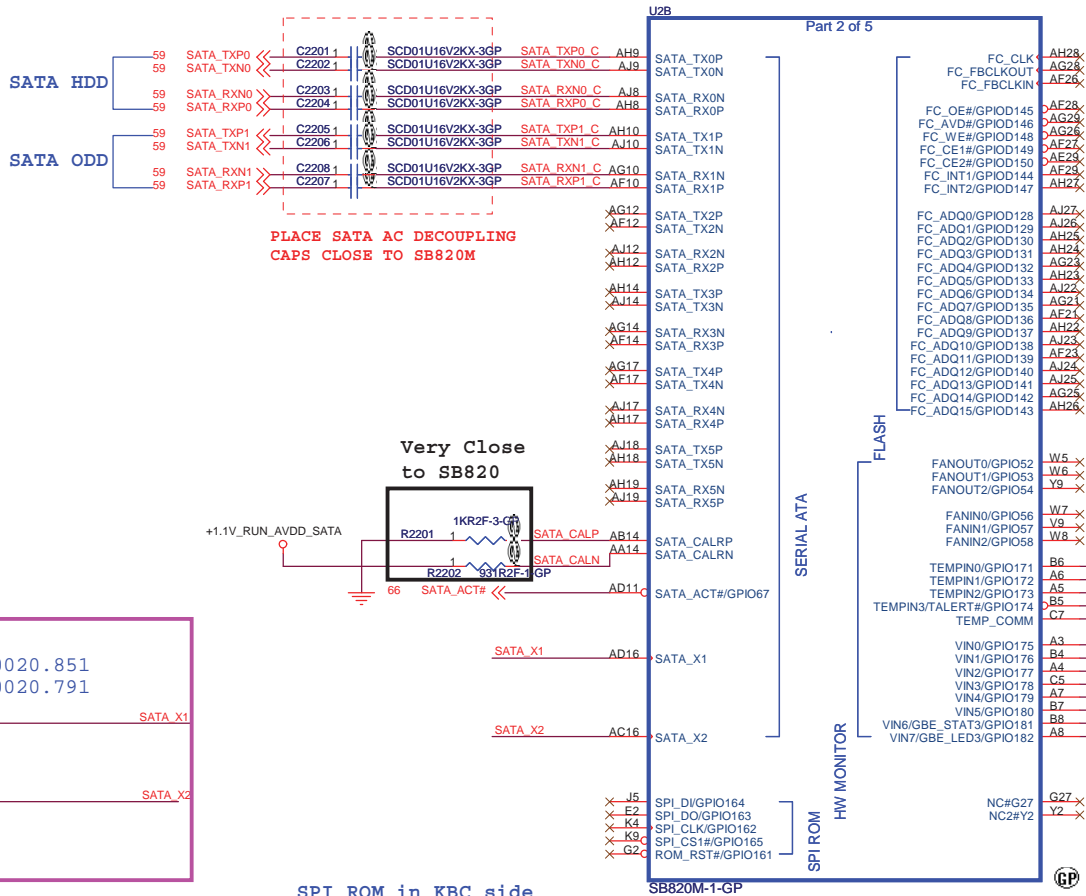
NOTE: SB8XX ONLY SUPPORTS 2 GPP
PORT 2 AND 3 IS NOT SUPPORTED. (From CRB)



Title **SB820M PCIE&PCI (1/5)**

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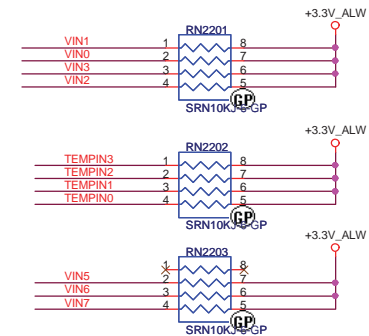


GPIO[150:128] are open drain GPIO pins where as GPO160 is an open drain GPO pin. These pins are not programmed to GPIO mode by default.

If use as GPIO, need to pull up to 1.8V_RUN

suggest not use HW monitor

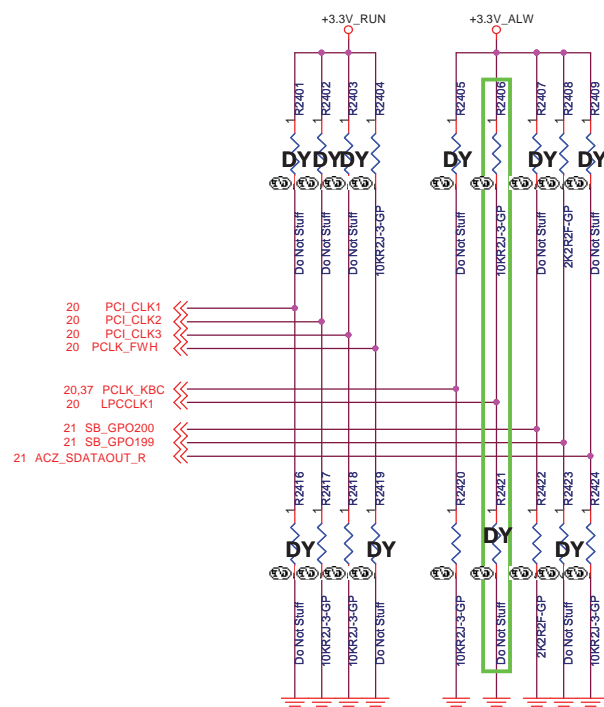
MEM_1V5 51



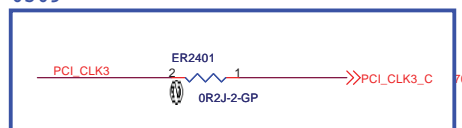
3 DJ2 AMD UMA (10-100 w HDMI)



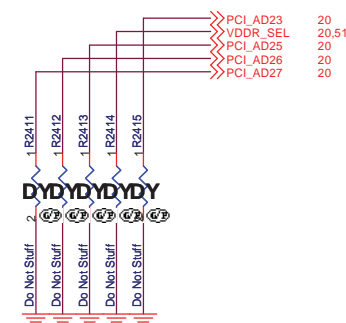
REQUIRED STRAPS



0309



DEBUG STRAPS



REQUIRED SYSTEM STRAPS

USE this pin to determine INT/EXT CLK

	AZ_SDOUT#	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCLK_FWH (PCI_CLK4)	PCLK_KBC (LPCCLK0)	LPCCLK1	SB_GPO200, SB_GPO199 ROM TYPE:
PULL HIGH	LOW POWER MODE	Allow PCIE GEN2 DEFAULT	WatchDOG (NB_PWRGD) ENABLED	USE DEBUG STRAPS	non_Fusion CLOCK mode DEFAULT	ENABLE EC	DEFAULT CLKGEN ENABLED (Use Internal)	H, H = Reserved H, L = SPI ROM
PULL LOW	PERFORMANCE MODE DEFAULT	Force PCIE GEN1	WatchDog (NB_PWRGD) DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT	Fusion CLOCK mode	DISABLE EC DEFAULT	CLKGEN DISABLED (Use External)	L, H = LPC ROM L, L = FWH ROM

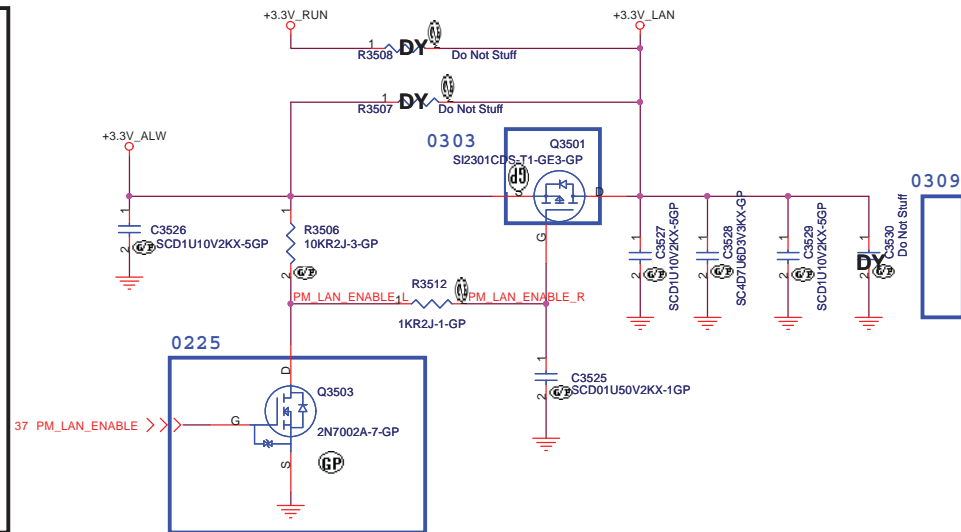
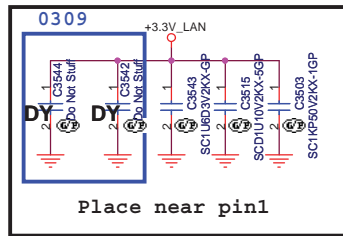
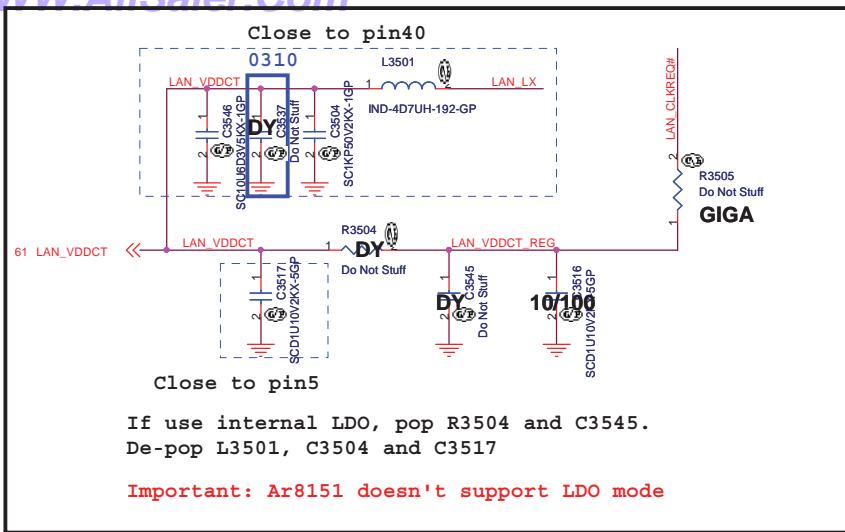
Not Applicable to SB820M
 but provision for pull-down is required.

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL (DEFAULT)	Disable ILA AUTORUN (DEFAULT)	USE FC PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)	Disable PCI MEM BOOT (DEFAULT)
PULL LOW	BYPASS PCI PLL	Enable ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	Enable PCI MEM BOOT

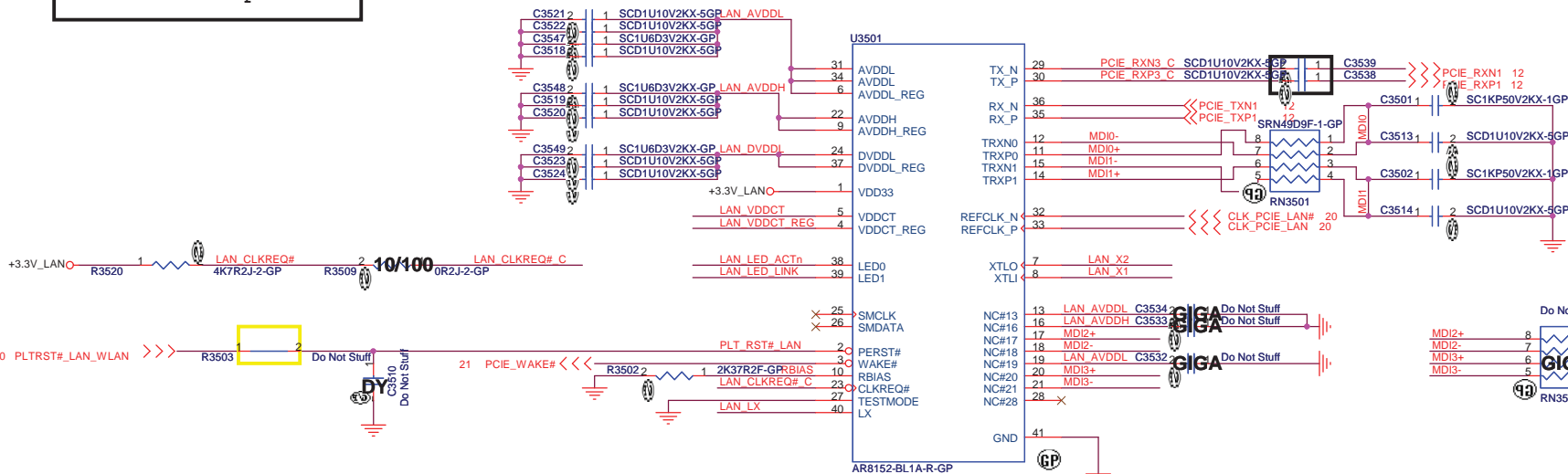
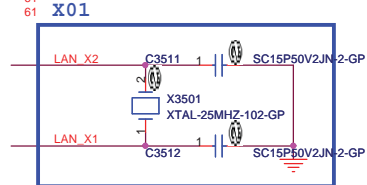
Note: SB820 has 15K internal PU FOR PCI_AD[27:23]



Title			
Card Reader-RTS5138			
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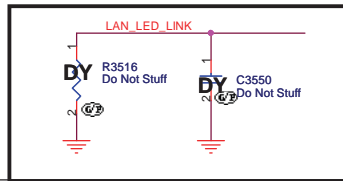
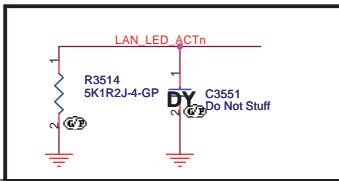
Pin6 is the AVDDL LDO output, 1uF+0.1uF(C3547 and C3518) close to Pin6;
C3522, C3521 close to Pin31, Pin34 respectively.
Pin9 is the AVDDH LDO output, 1uF+0.1uF(C3548 and C3519) close to Pin9;
C3520 close to Pin22.
Pin37 is the DVDDL LDO output, 1uF+0.1uF(C3549 and C3523) close to Pin37;
C3524 close to Pin24.



If overclocking, de-pop R3514 and C3551

If use LDO mode, pop R3516 and C3550

GIGA LAN use 71.08151.003



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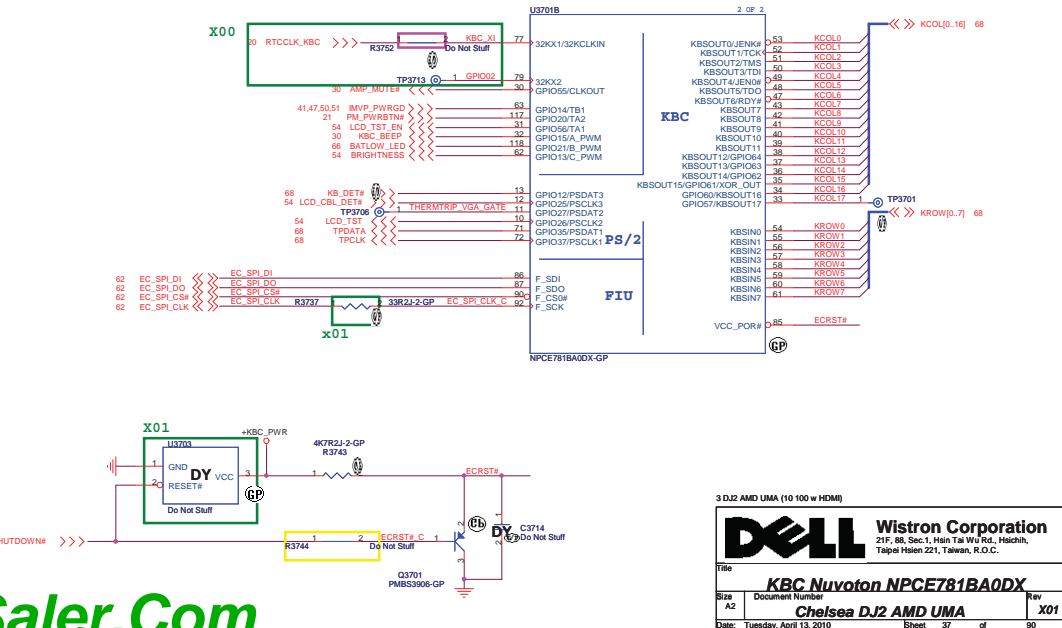
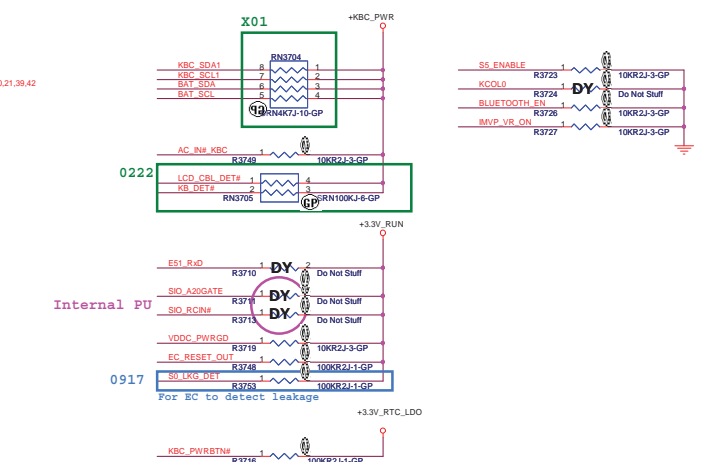
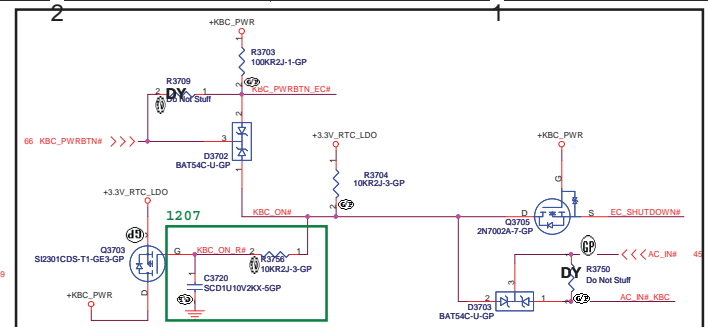
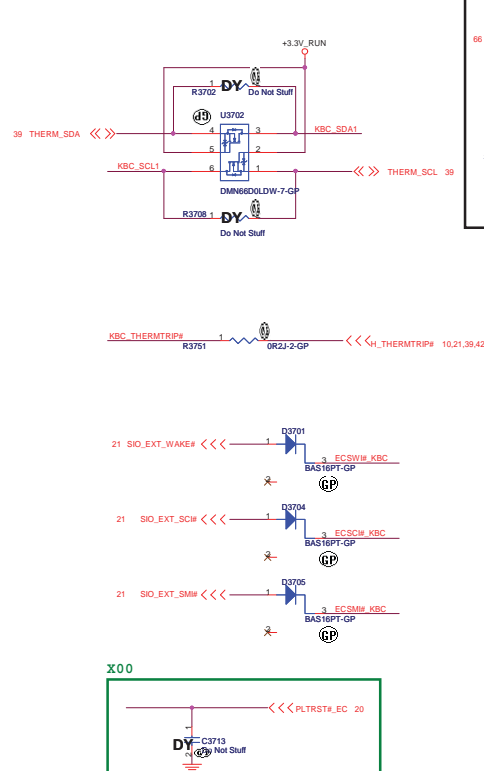
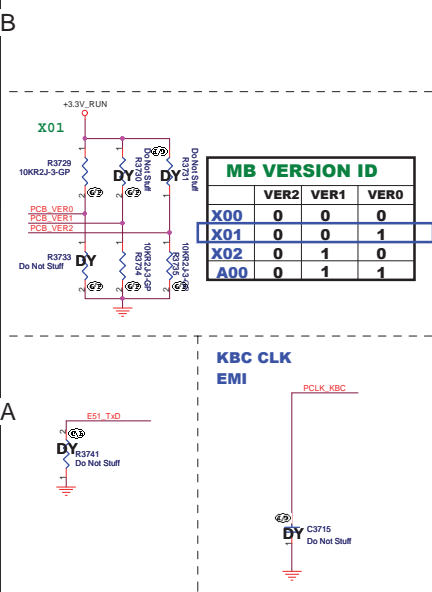
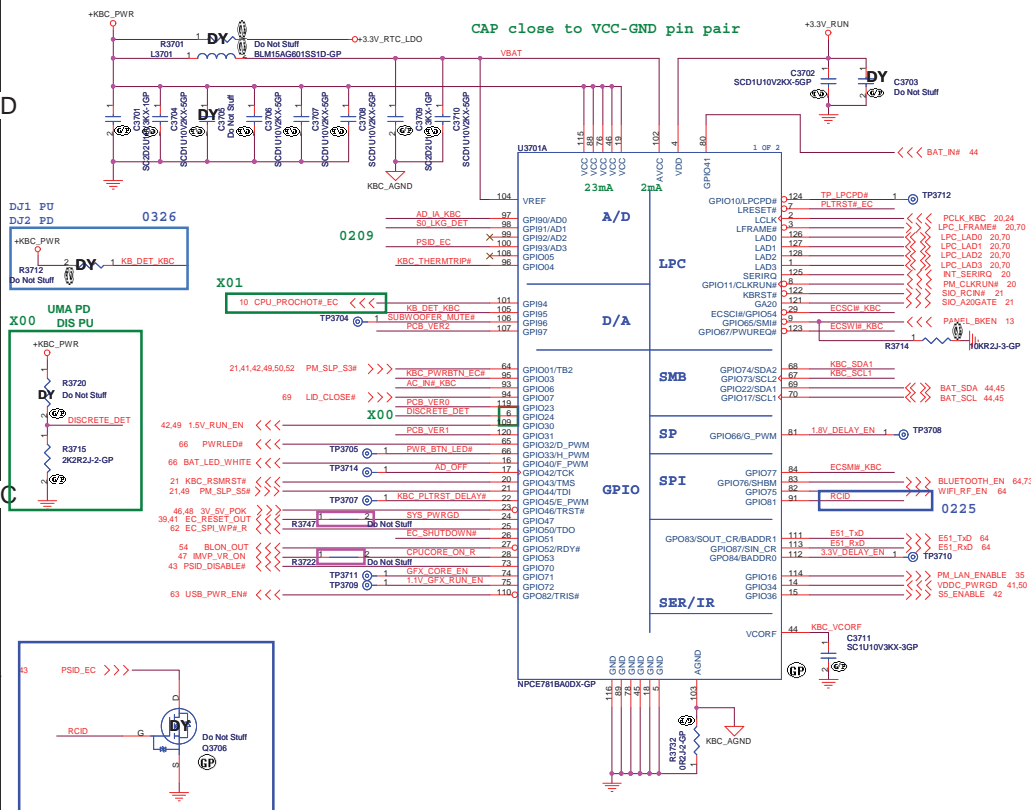
DELL Wistron Corporation

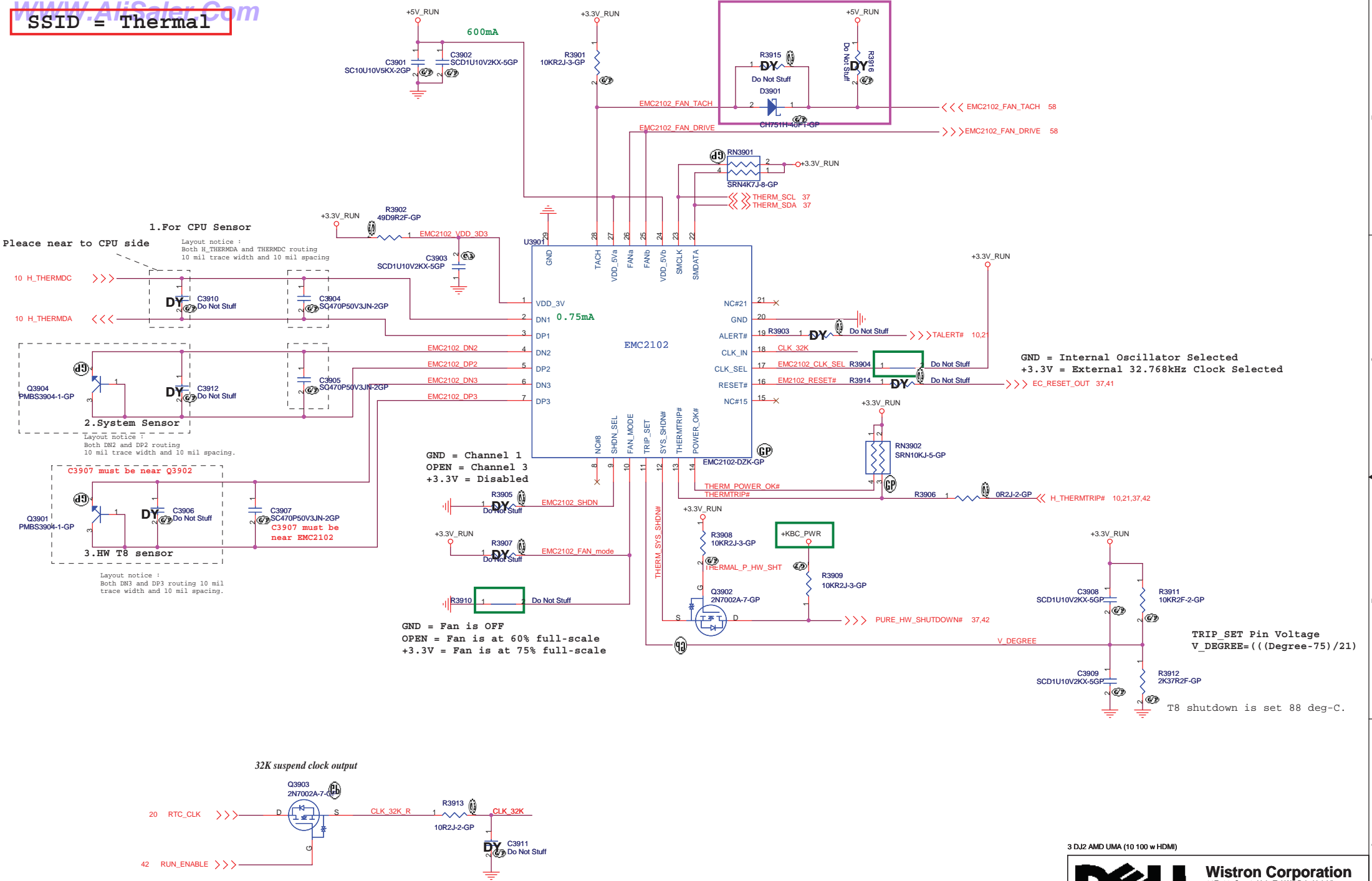
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title **AR8152/AR8151**

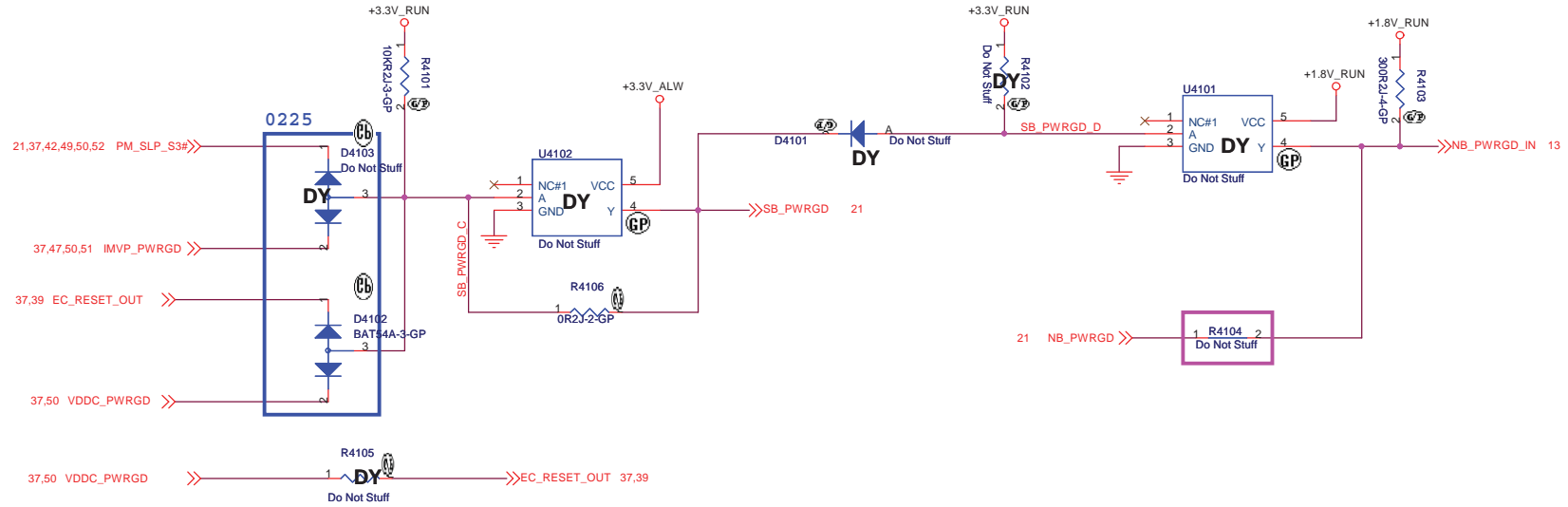
Size A3 Document Number **Chelsea DJ2 AMD UMA** Rev **X01**

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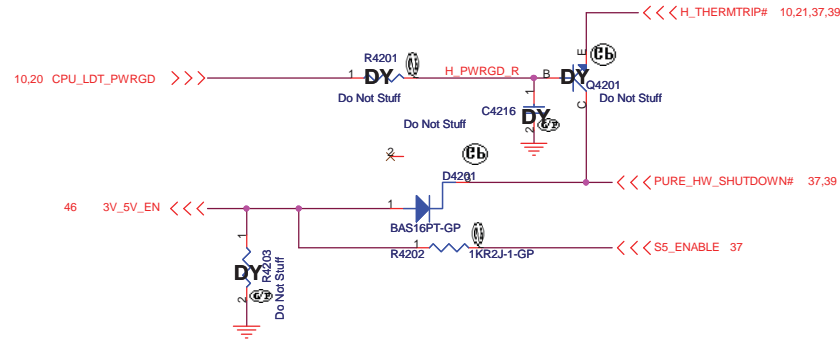
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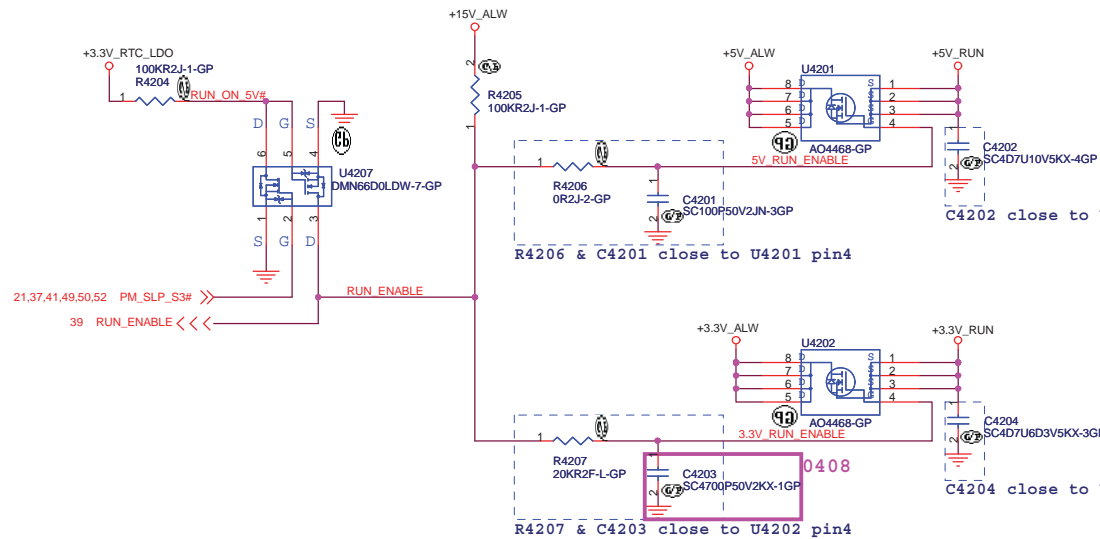
3 DJ2 AMD UMA (10 100 w HDMI)

DELL		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Power On Logic			
Size A3	Document Number	Rev	
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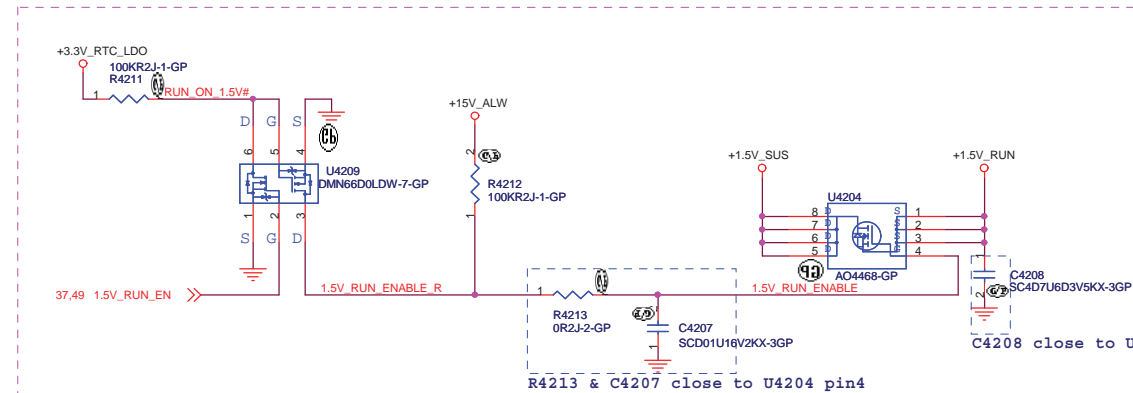
SSID = Reset.Suspend



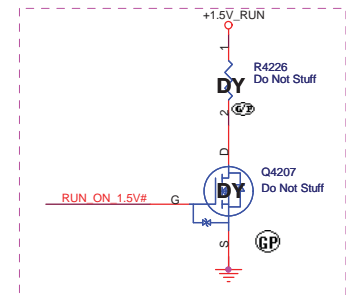
Run Power



Peak current: 6257.3mA (HD:1100 ODD:2500)
Design current: 4380.11 mA
11.6A
Rds=14m ohm



Peak current: 1230mA
Design current: 861 mA
11.6A
Rds=14m ohm



3 DJ2 AMD UMA (10 100 w HDMI)

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			Power Plane Enable	
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DCIN

Chelsea DJ2 AMD UMA

Rev
Y01

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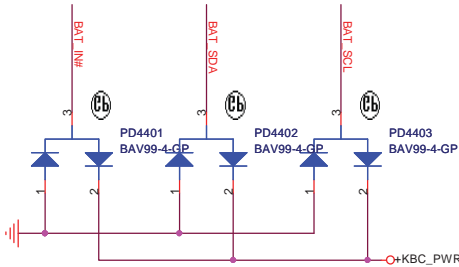
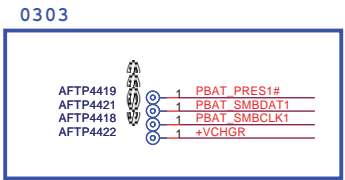
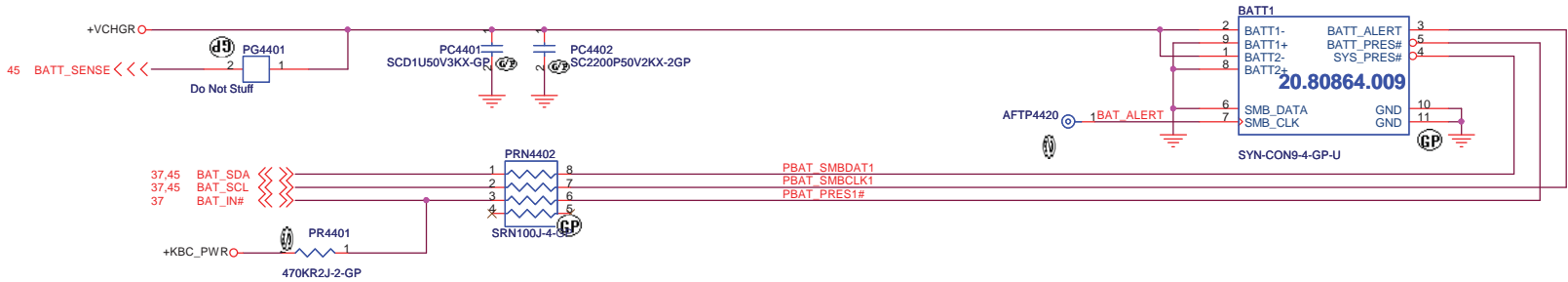
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Batt Connector



3 DJ2 AMD UMA (10 100 w HDMI)



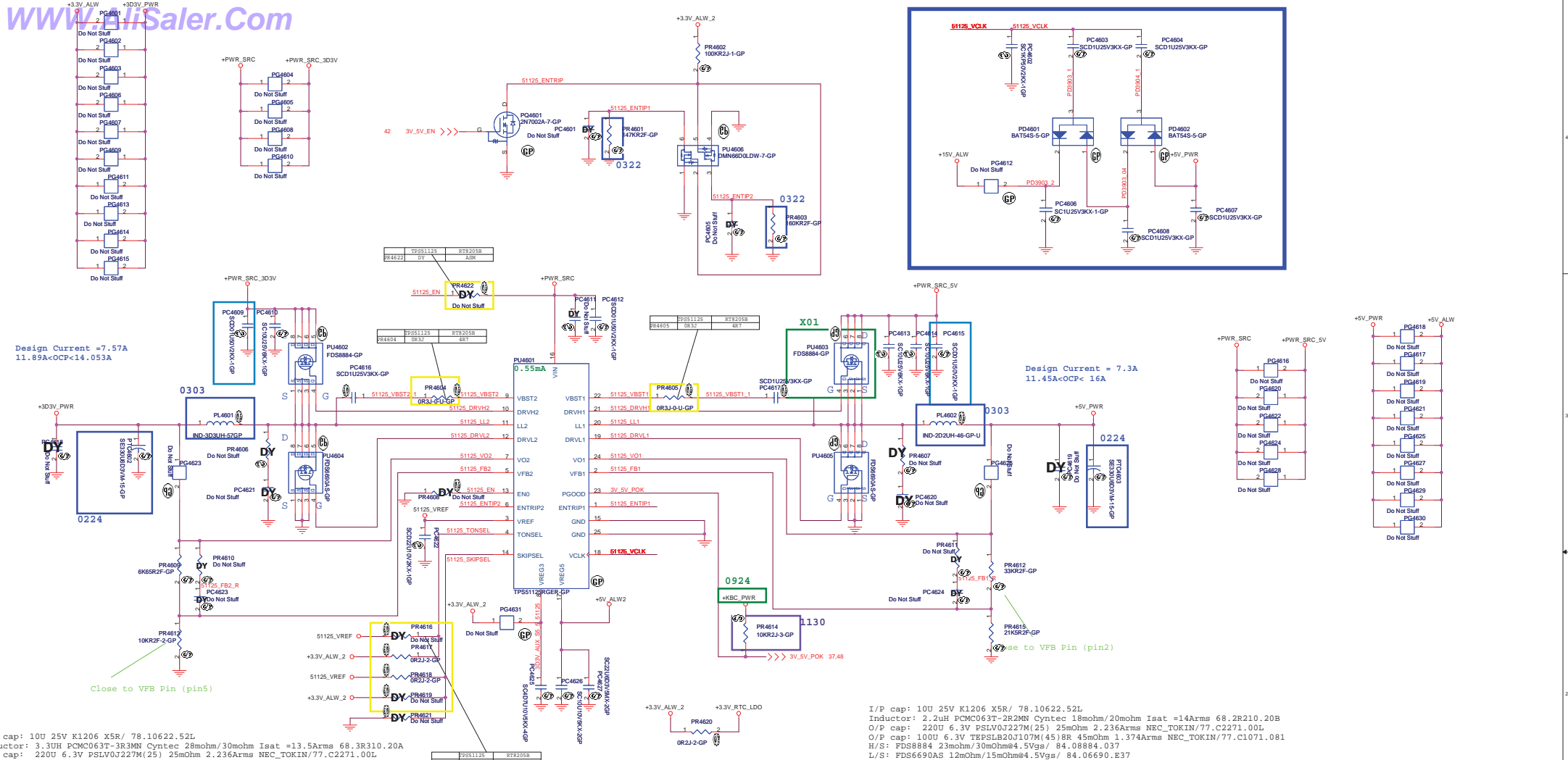
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title **BATT CONN**

Size A3 Document Number **Chelsea DJ2 AMD UMA** Rev **X01**

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TPS51125 74.08205.A731:

TONSEL	CH1	CH2
GND	200kHz	265kHz
VREF	245kHz	305kHz
VRBG3	300kHz	375kHz
VRBG5	365kHz	460kHz

TPS51125 74.08205.B731:

TONSEL	CH1	CH2
GND	200kHz	250kHz
VREF	300kHz	375kHz
VRBG3	365kHz	460kHz
VRBG5	365kHz	460kHz

TPS51125 74.51125.073

RT8205BQW	74.08205.B73
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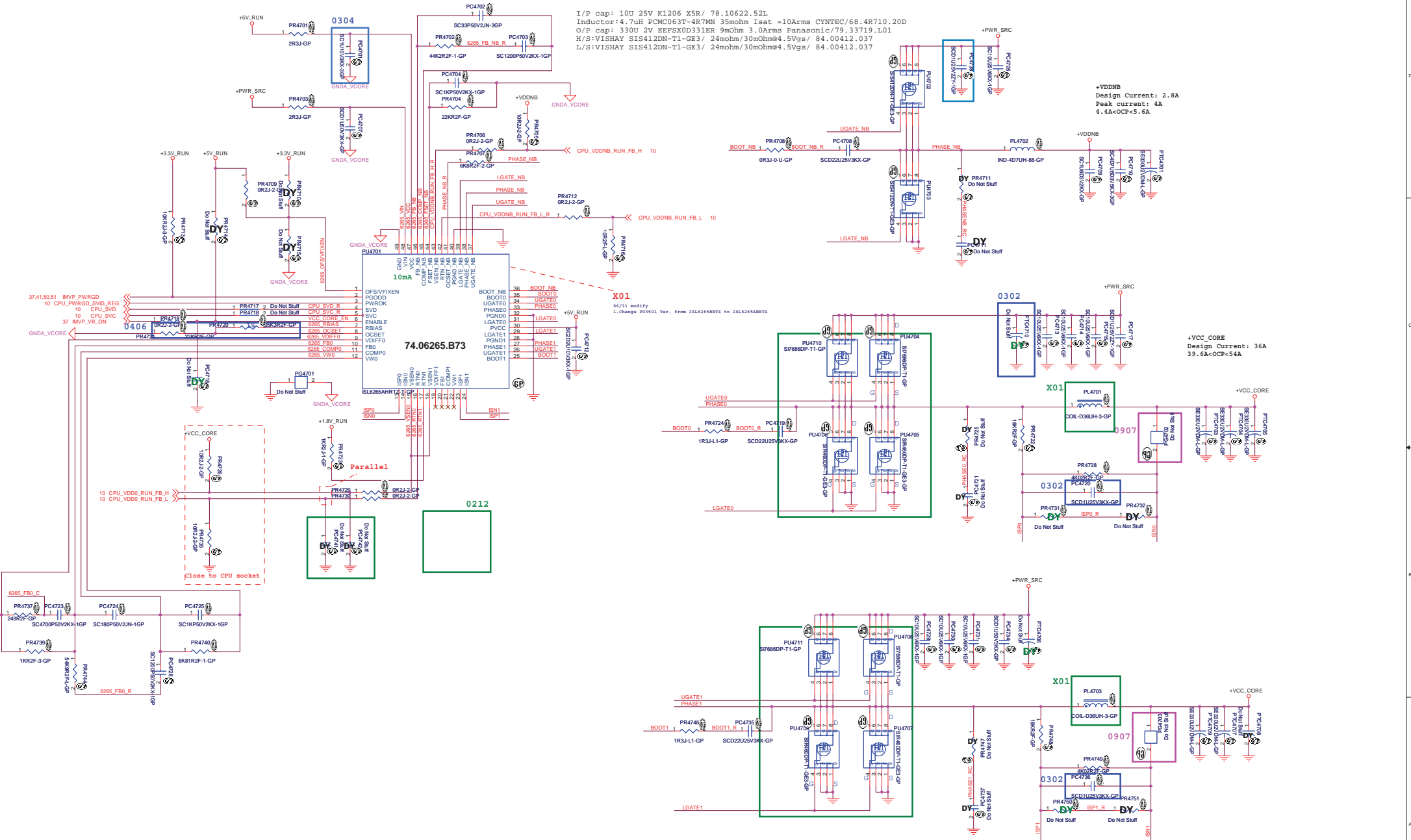
SKIPSEL	VREG3 or VRBG5	VREF (2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

EN0	Open	820k to GND	GND
Operating Mode	enable both LDOs, VCLK on and ready to turn on switcher channels	enable both LDOs, VCLK off and ready to turn on switcher channels	disable all circuit

3 DJ2 AMD UMA (10 100 w HDMI)

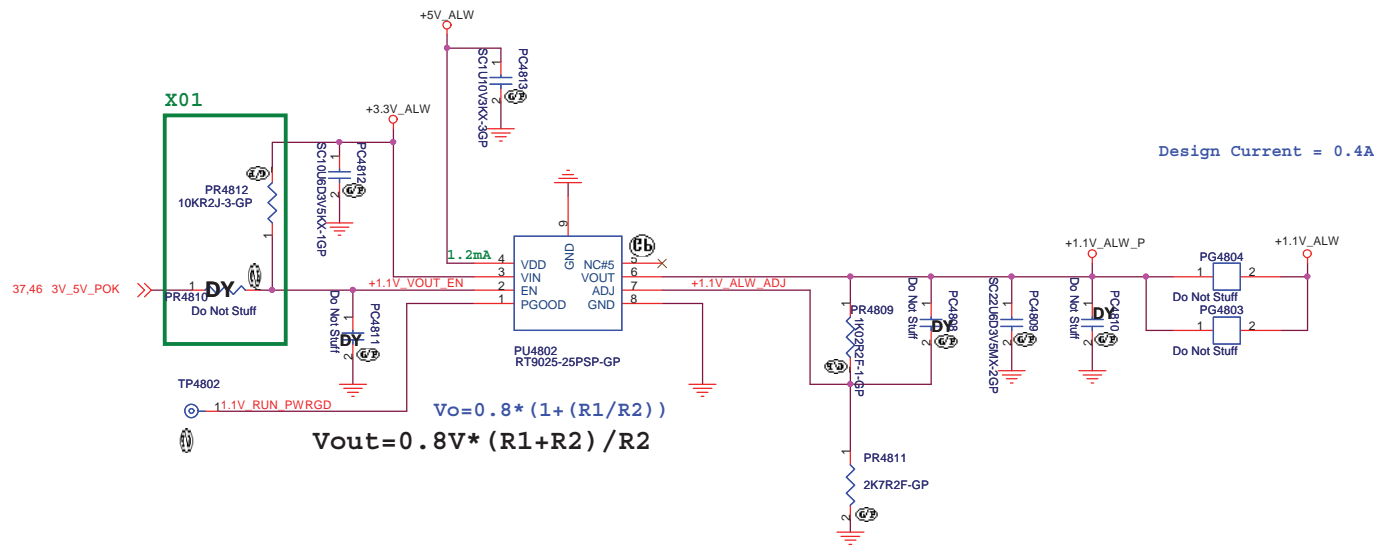
DELL Wistron Corporation	
21F, 8th, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: TPS51125 5V/3D3V	
Size: A2	Document Number: Cheslea DJ2 AMD UMA
Date: Tuesday, April 13, 2010	Sheet: 46 of 90

ISL6265HRTZ-T for +VCC_CORE&+VDDNB



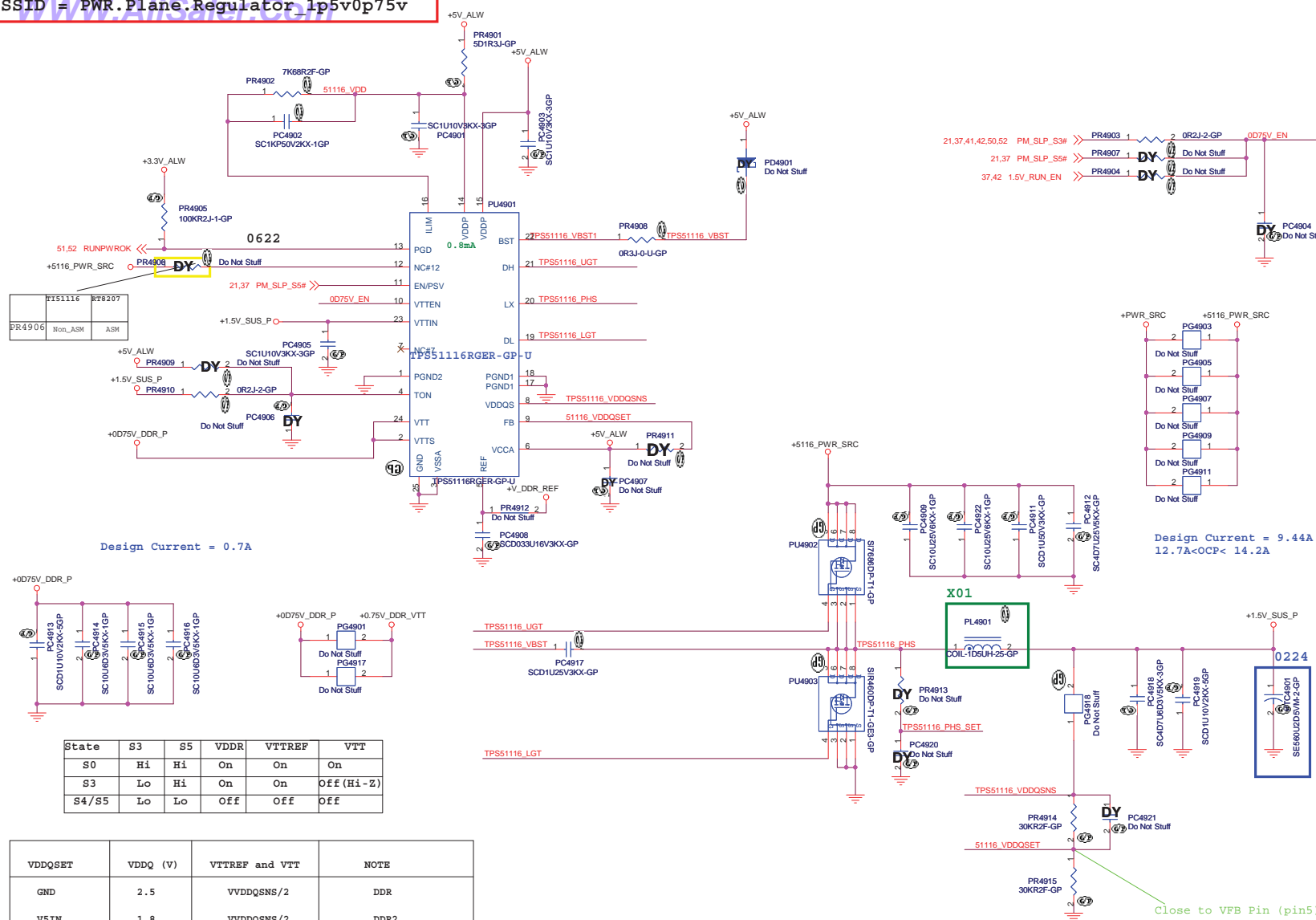
SSID = PWR.Plane.Regulator_+1.1V_RUN

RT9025 for +1.1V_ALW



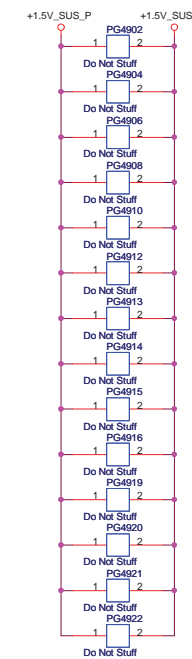
3 DJ2 AMD UMA (10 100 w HDMI)

DELL		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title RT9025_+1.1VALW			
Size A3	Document Number Chelsea DJ2 AMD UMA	Rev X01	
Date: Tuesday, April 13, 2010	Sheet 48 of 90		



VDDQSET	VDDQ (V)	VTTREF and VTT	NOTE
GND	2.5	VVDDQSNS/2	DDR
V5IN	1.8	VVDDQSNS/2	DDR2
FB Resistors	Adjustable	VVDDQSNS/2	1.5 V < VVDDQ < 3 V

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.5UHPCCMI04T-IR5M DCr/3.8/4.2mohm Isat =33Arms Cyntec/ 68.1R510.10.
O/P cap: 220U 2V EFXCD0D221R 150hm 2.7Arms PANASONIC/ 79.22719.20L
H/S: PDS8880 9.6mohm/12mohm4.5VgS/ 84.08880.037
L/S: PDS6676AS 5.9mohm/7.25mohm4.5VgS/ 84.06676.A37



3 DJ2 AMD UMA (10 100 w HDMI)

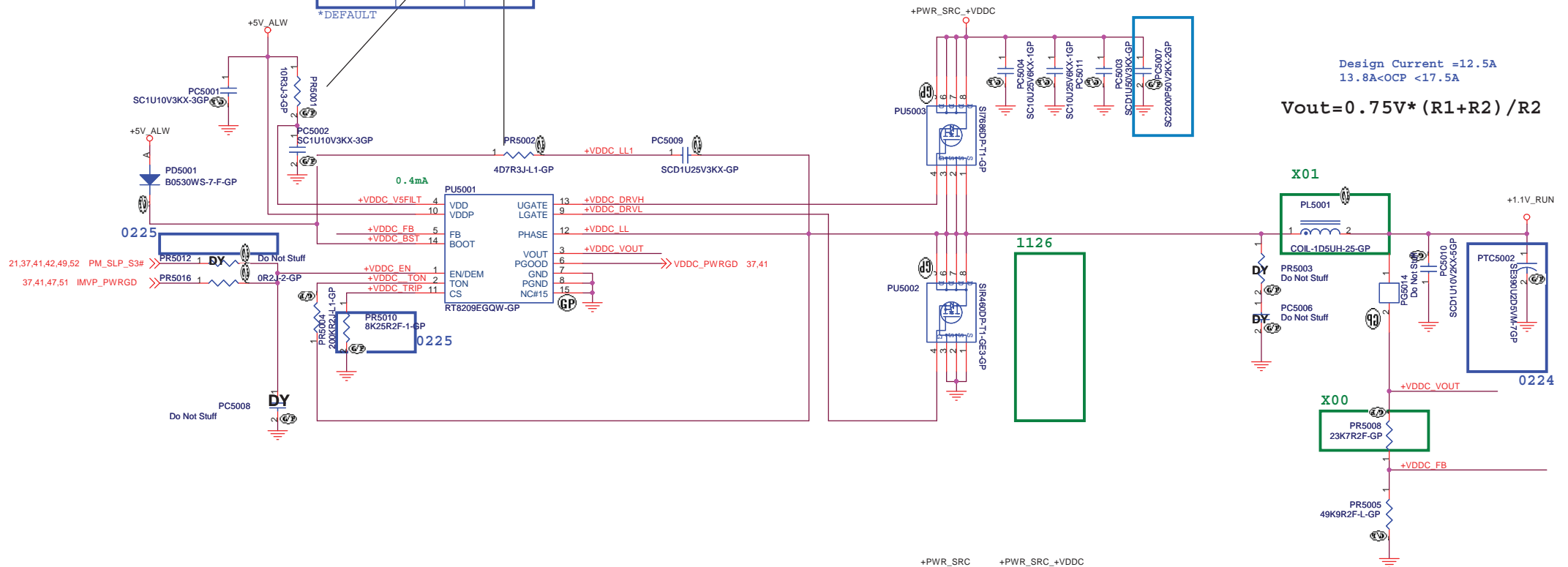


Title			
TPS51116RGER +1.5V SUS			
Size	Document Number	Rev	
Custom	Chelsea DJ2 AMD UMA	X01	
Date:	Tuesday, April 13, 2010	Sheet 49	of 90

SSID = PWR.Plane.Regulator_VDDC

PWM TYPE	PR5001	PR5002
*RT8209E	10 ohm	4.7 ohm
TPS51117	300 ohm	0 ohm

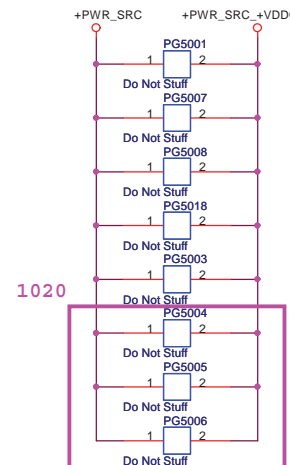
*DEFAULT



Design Current =12.5A
13.8A<OCP <17.5A

$$V_{out}=0.75V \cdot (R1+R2) / R2$$

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.5UHPCMC104T-1R5MN DCR:3.8/4.2mohm Isat =33Arms Cyntec/ 68.1R510.10
O/P cap: 330U 2.5V PSLV0E337M(15) 15mOhm 2.886Arms NEC_TOKIN/ 77.C3371.10L
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: SiR460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037



3 DJ2 AMD UMA (10 100 w HDMI)

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

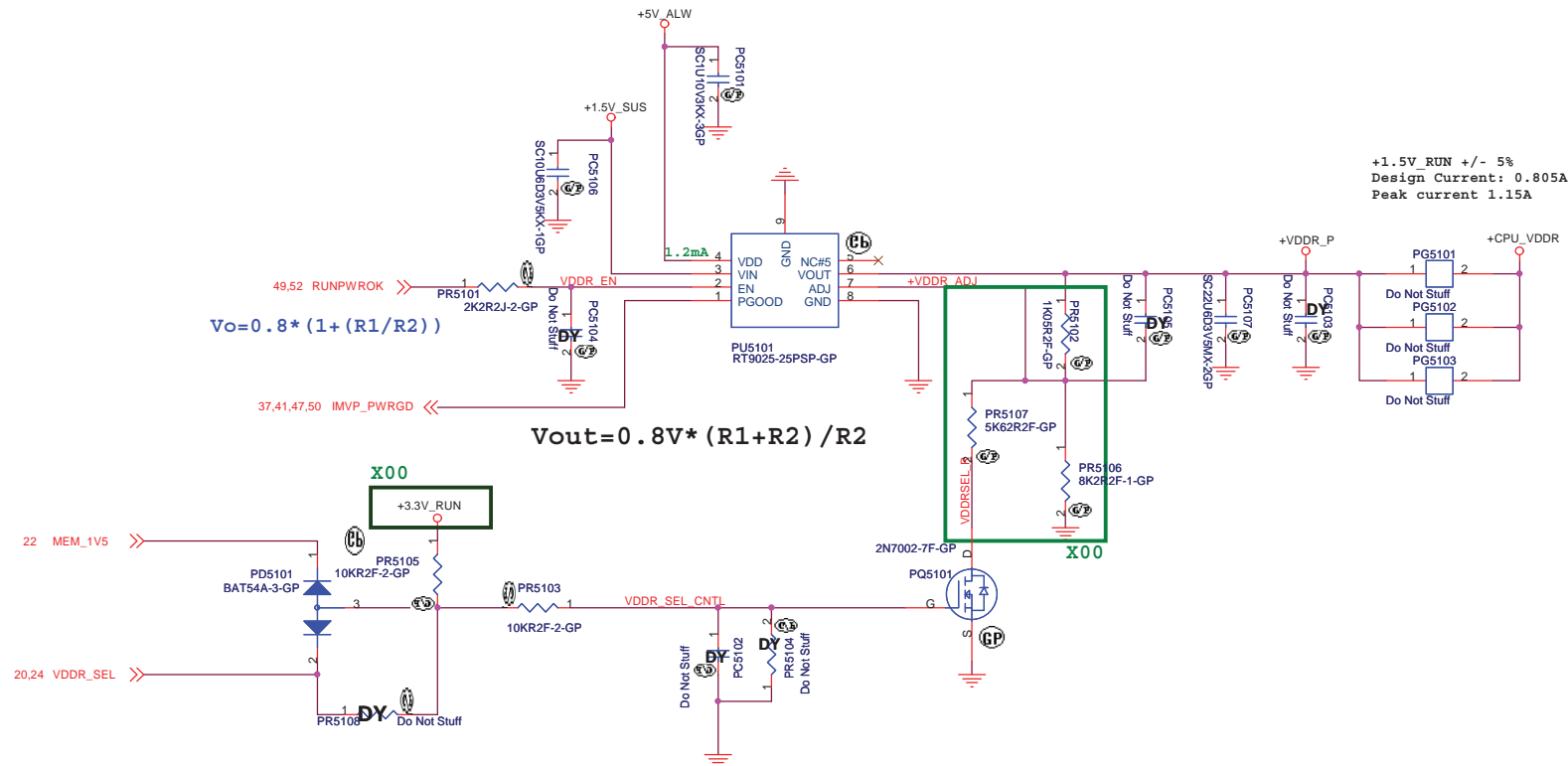
Title
RT8209 +1.1V RUN

Size A3 Document Number
Chelsea DJ2 AMD UMA

Date: Tuesday, April 13, 2010 Sheet 50 of 90

Rev
X01

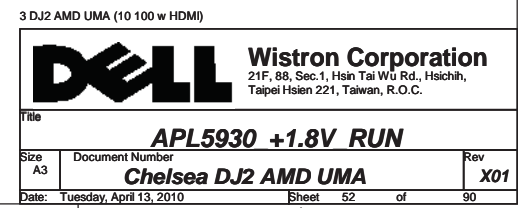
RT9025 for +VDDR



VDDR_SEL	+CPU_VDDR
H	1.05V
L	0.9V

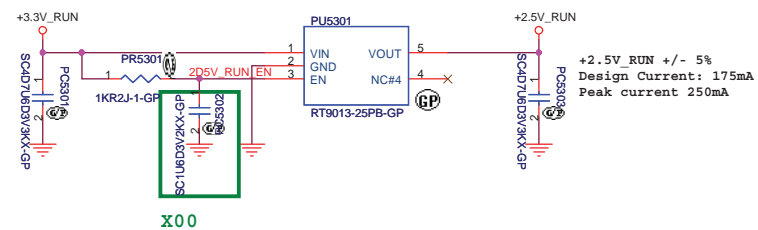
3 DJ2 AMD UMA (10 100 w HDMI)

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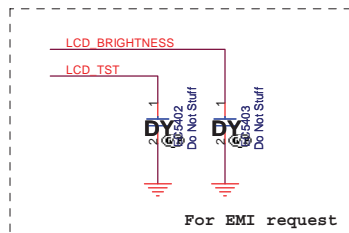
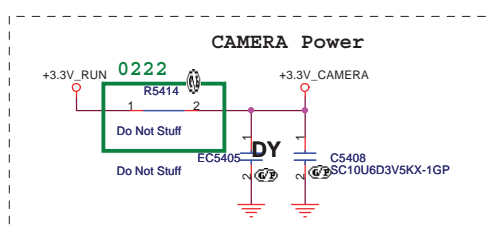
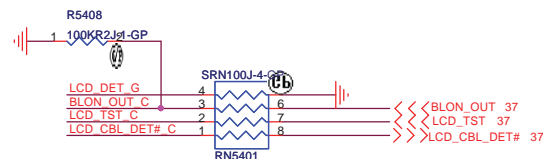
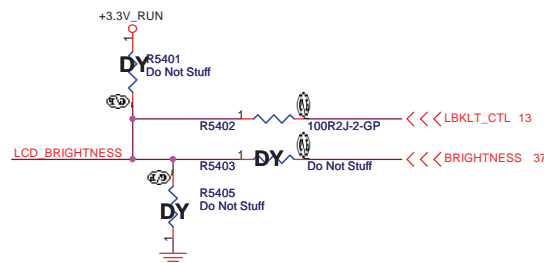
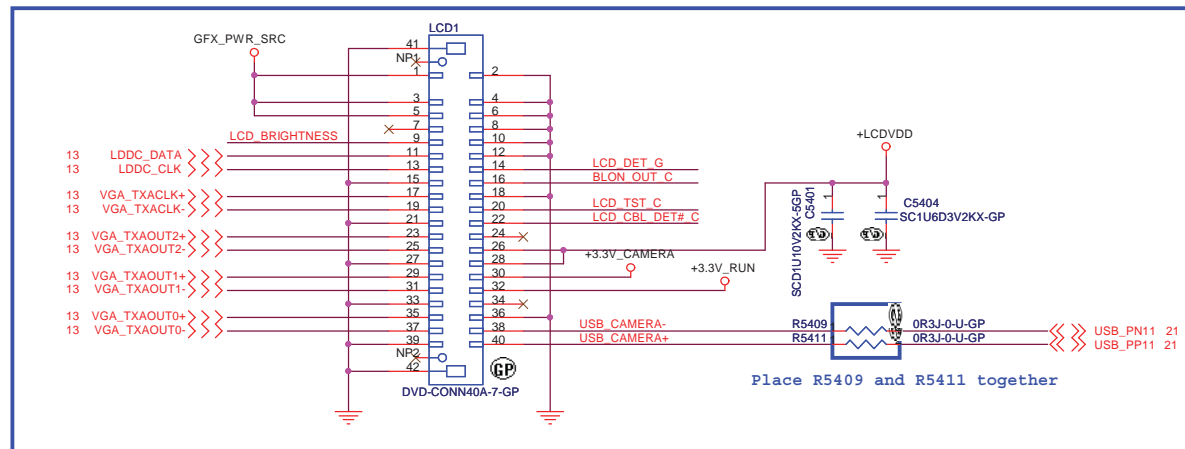
SSID = PWR.Plane.Regulator_2p5v

RT9013-25PB for +2.5V_RUN



LVDS CONNECTOR

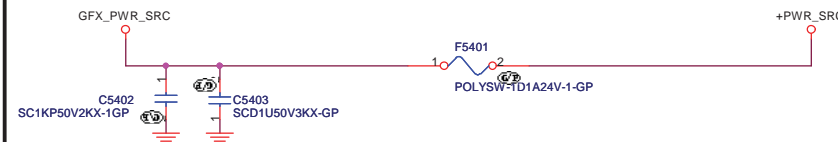
0225



For EMI request

SSID = Inverter

INVERTER POWER

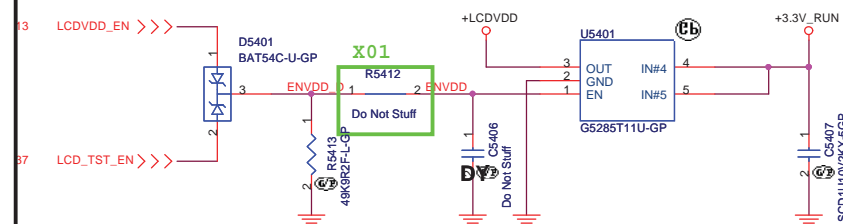


0224



SSID = VIDEO

LCD POWER



3 DJ2 AMD UMA (10 100 w HDMI)

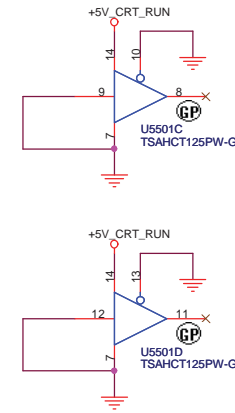
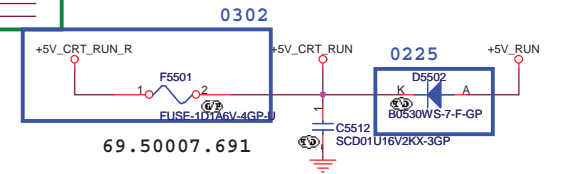
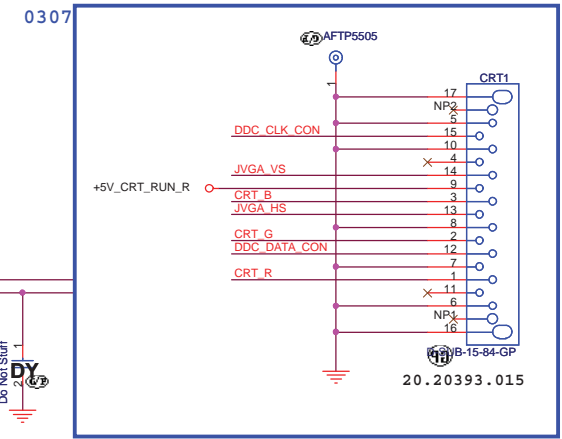
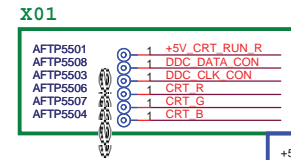
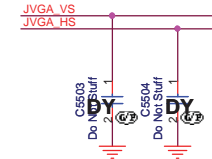
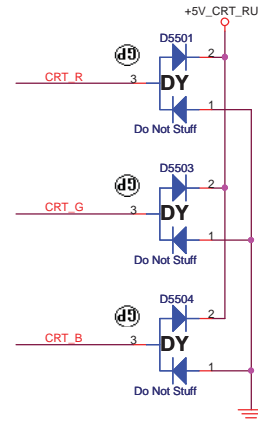
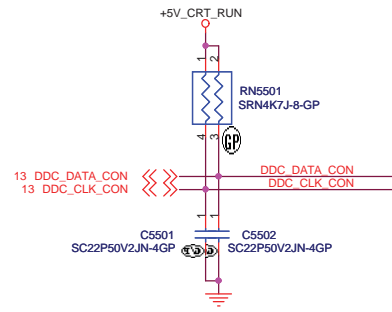
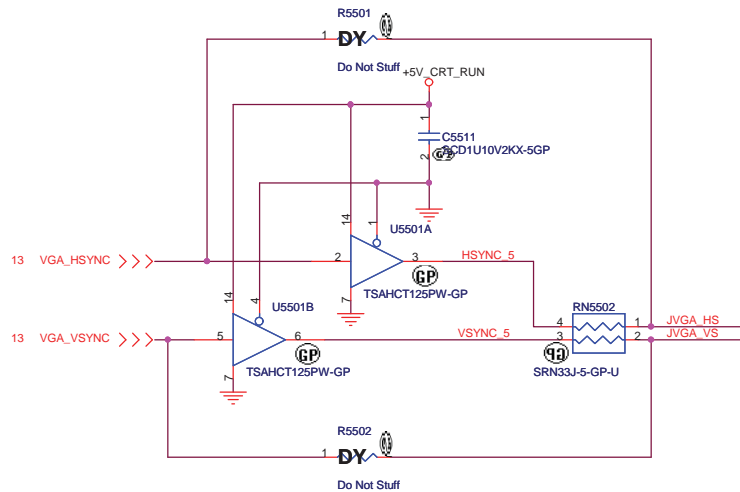
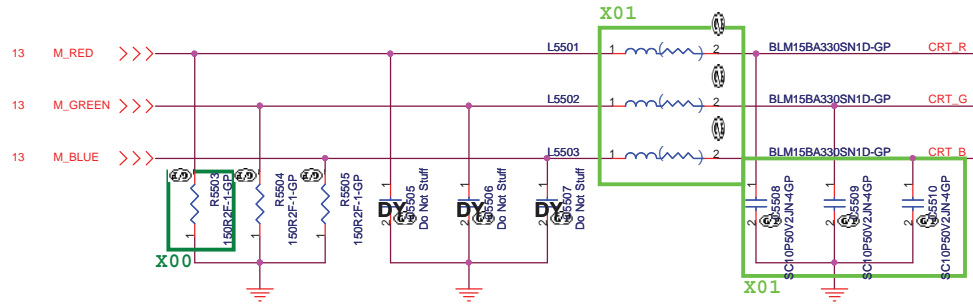
DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

LCD/Inverter Connector			
Size	Document Number	Rev	
A3	Chelsea DJ2 AMD UMA	X01	
Date:	Tuesday, April 13, 2010	Sheet	54 of 90

SSID = VIDEO

Layout Note:

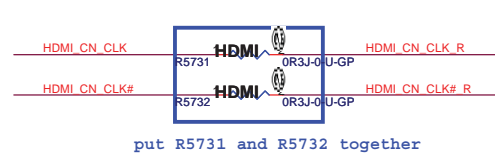
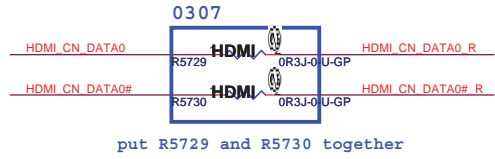
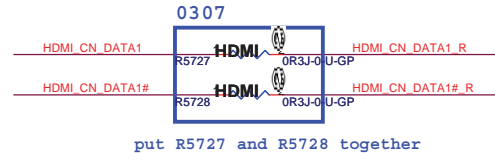
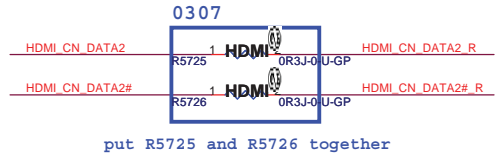
- *Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN.
- * RGB signal will hit 75 Ohm first, then pi-filter, finally CRT CONN.



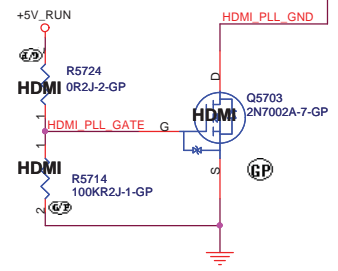
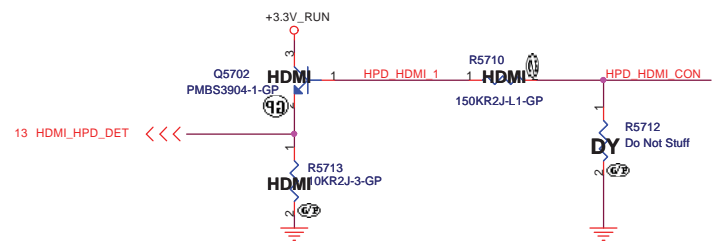
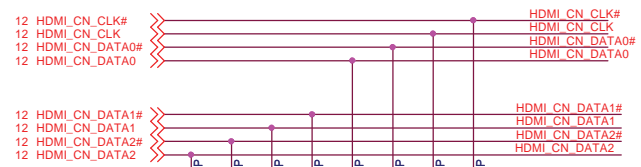
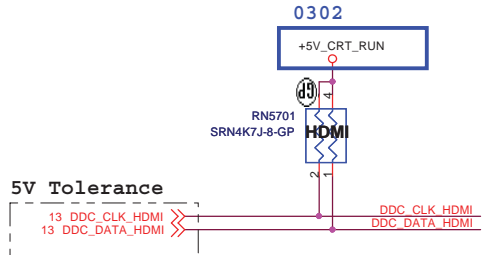
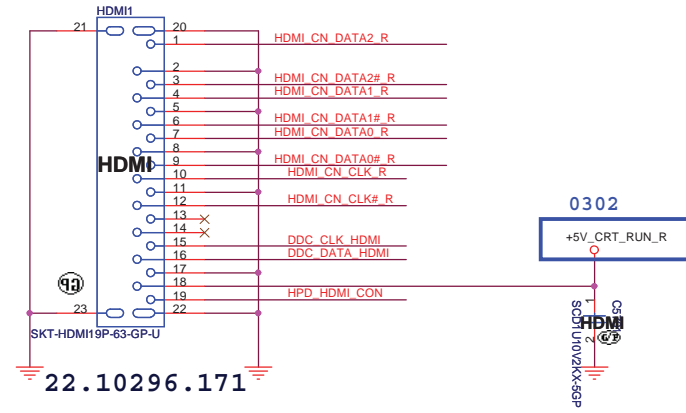
3 DJ2 AMD UMA (10 100 w HDMI)

SSID = VIDEO

HDMI CONNECTOR



HDMI CONN

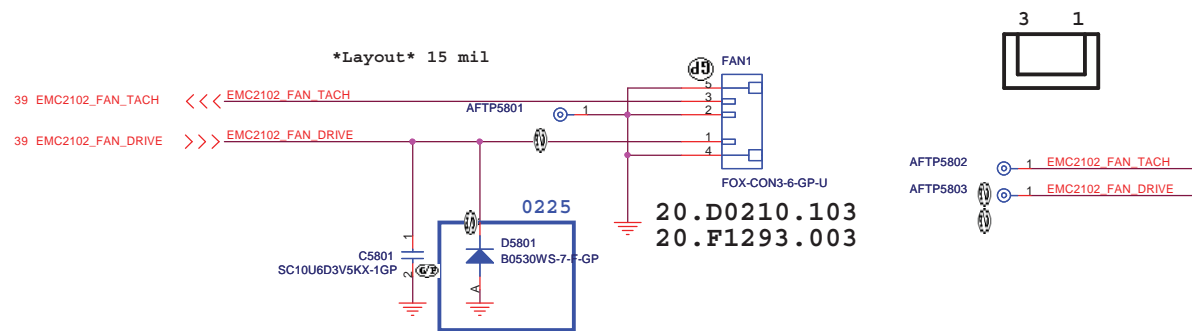


3 DJ2 AMD UMA (10 100 w HDMI)

DELL		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title: HDMI Level Shifter/Connector			
Size: A3	Document Number: Chelsea DJ2 AMD UMA	Rev: X01	
Date: Tuesday, April 13, 2010	Sheet: 57	of: 90	

SSID = Thermal

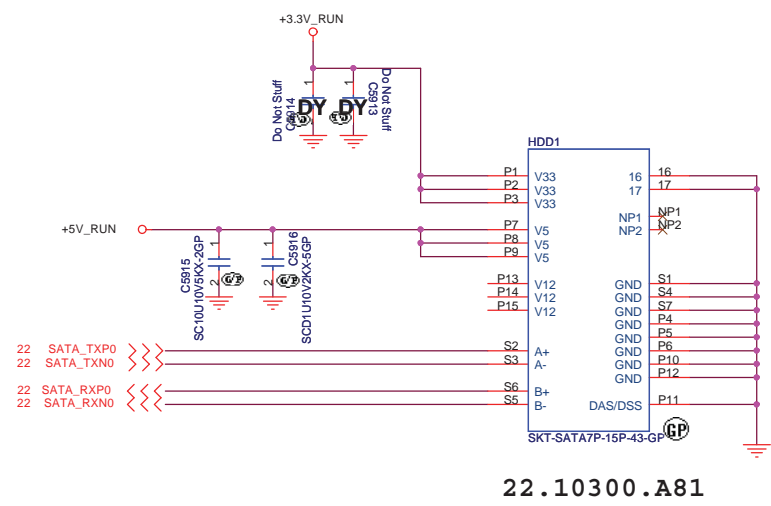
Fan Connector



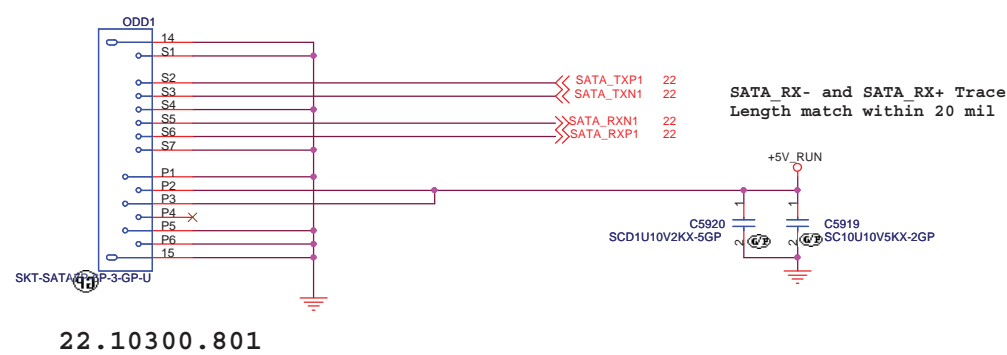
3 DJ2 AMD UMA (10 100 w HDMI)

DELL		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
ITP/Fan Connector			
Size	Document Number	Rev	
A3	Chelsea DJ2 AMD UMA	X01	
Date:	Tuesday, April 13, 2010	Sheet	58 of 90

SATA HDD Connector

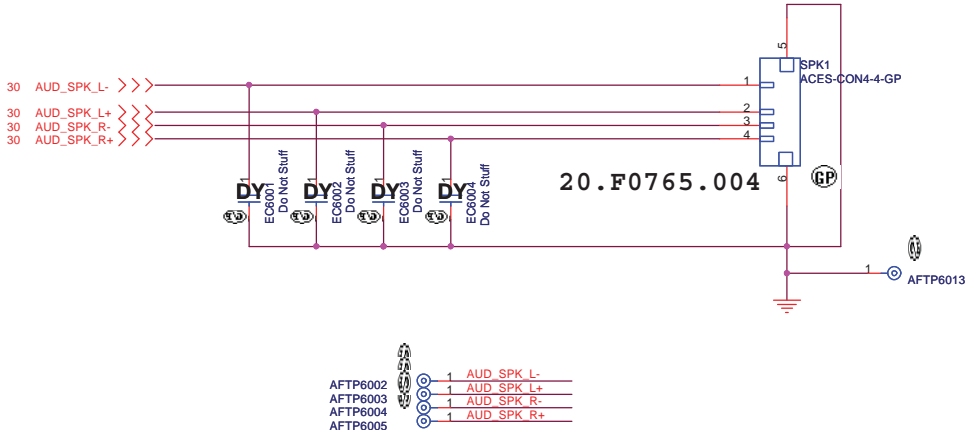


ODD Connector

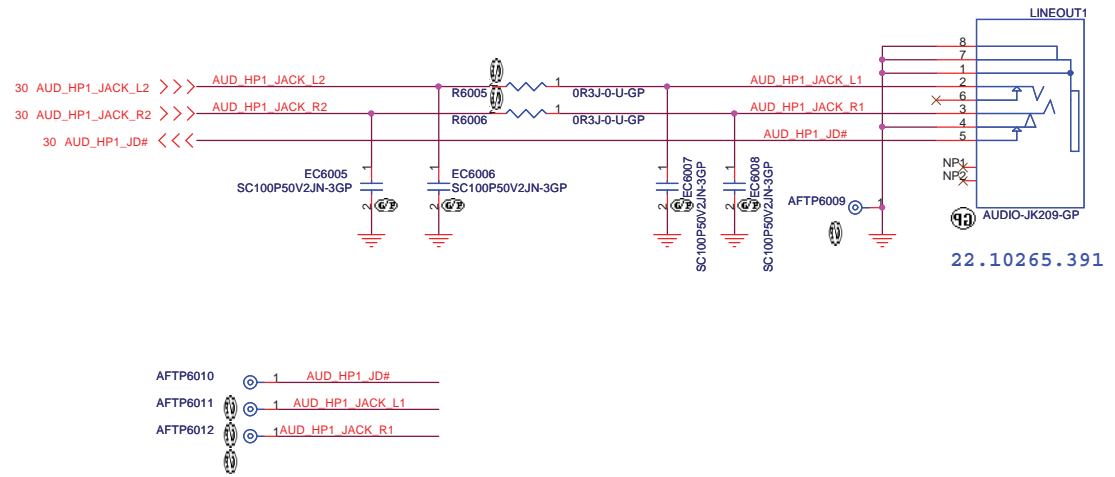


3 DJ2 AMD UMA (10 100 w HDMI)

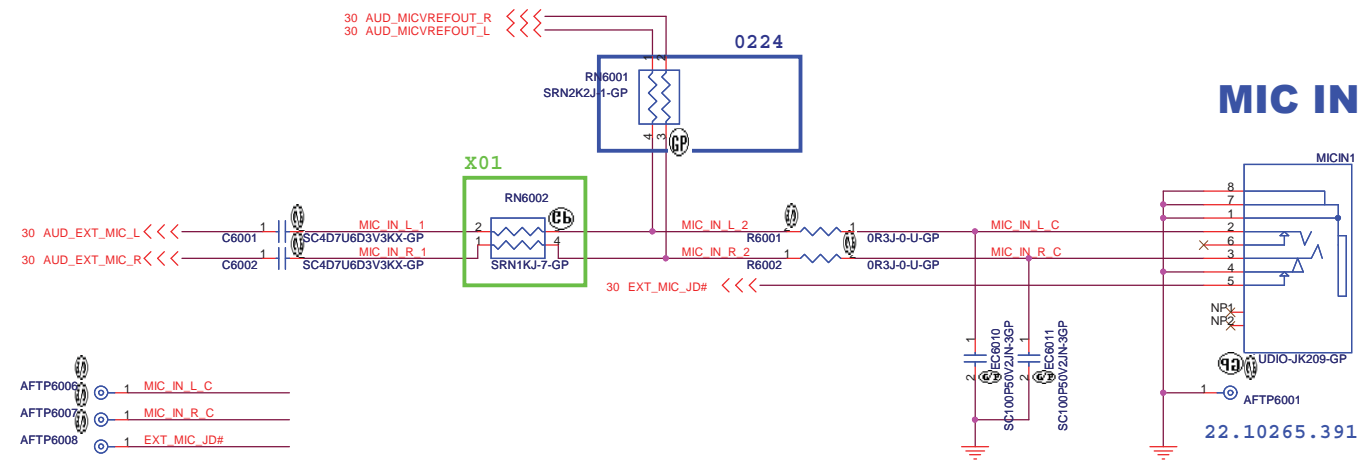
Speaker Connector



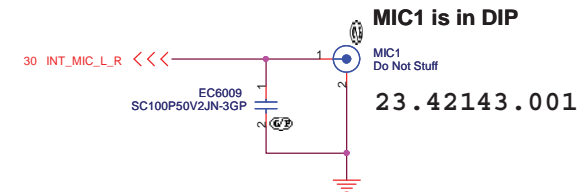
LINE1 OUT



MIC IN



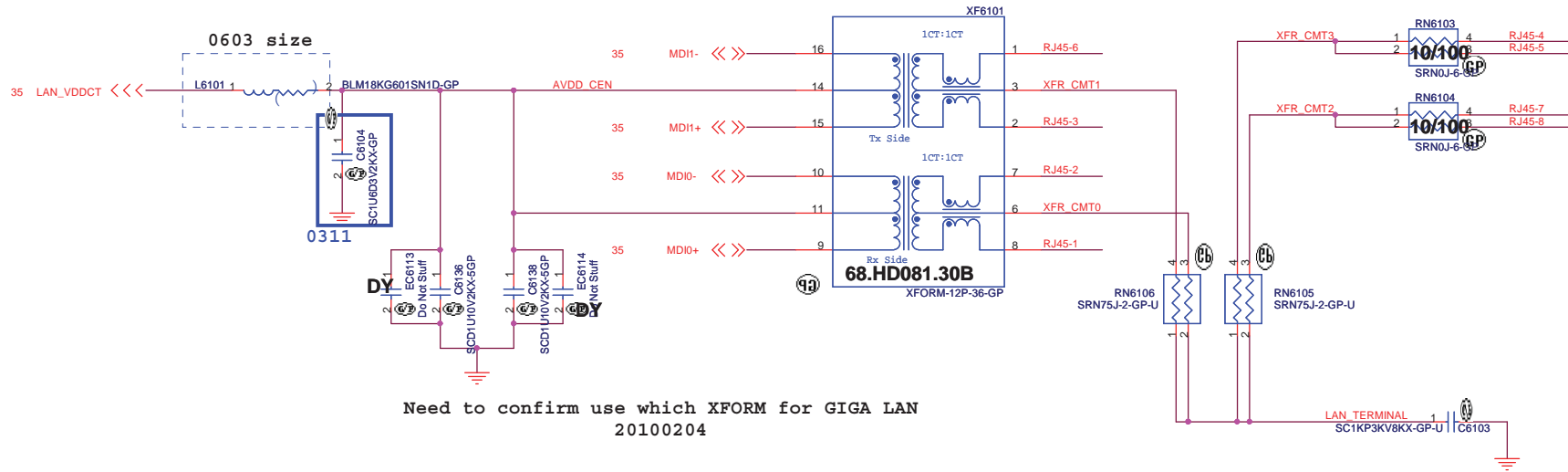
Internal Microphone



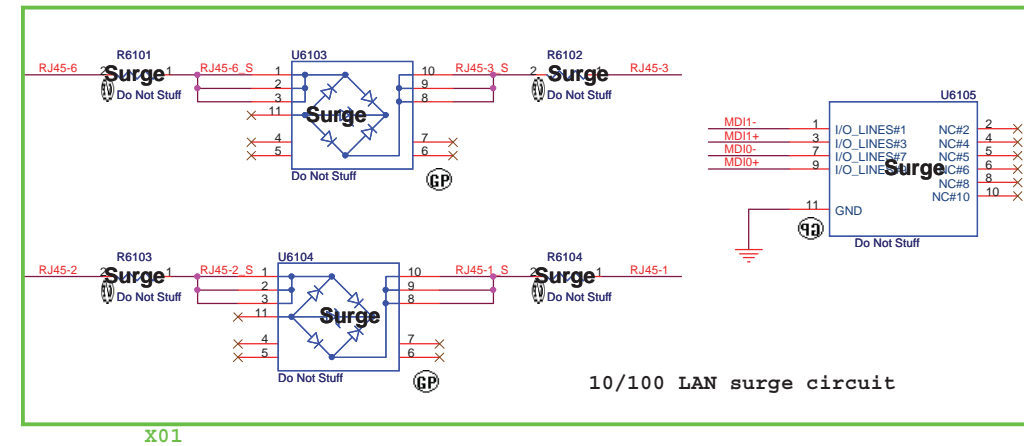
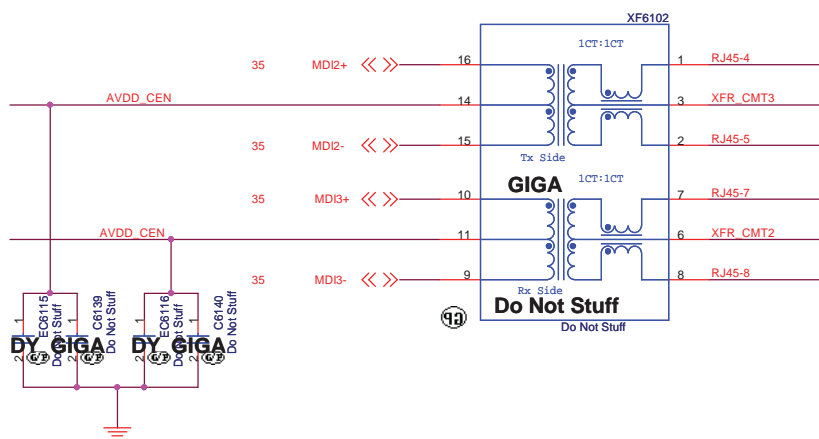
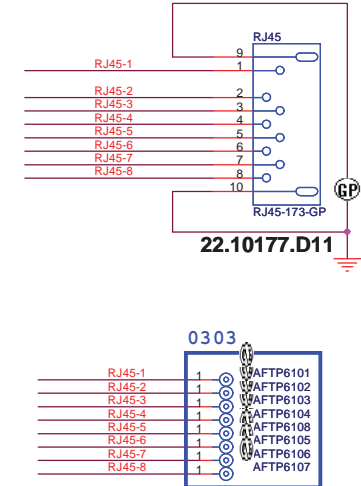
2009-10-1 Change MDI1+ (XF601.16) to MDI1+ (XF601.15)
 Change MDI1- (XF601.15) to MDI1- (XF601.16)
 Change MDI0+ (XF601.10) to MDI0+ (XF601.9)
 Change MDI0- (XF601.9) to MDI0- (XF601.10)
 Change RJ45-3 (XF601.1) to RJ45-3 (XF601.2)
 Change RJ45-6 (XF601.2) to RJ45-6 (XF601.1)
 Change RJ45-1 (XF601.7) to RJ45-1 (XF601.8)
 Change RJ45-2 (XF601.8) to RJ45-2 (XF601.7)

1. route on bottom as differential pairs.
2. Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3. No vias, No 90 degree bends.
4. pairs must be equal lengths.
5. 6mil trace width, 12mil separation.
6. 36mil between pairs and any other trace.
7. Must not cross ground moat, except RJ-45 moat.

10/100M Lan Transformer



RJ45 Connector



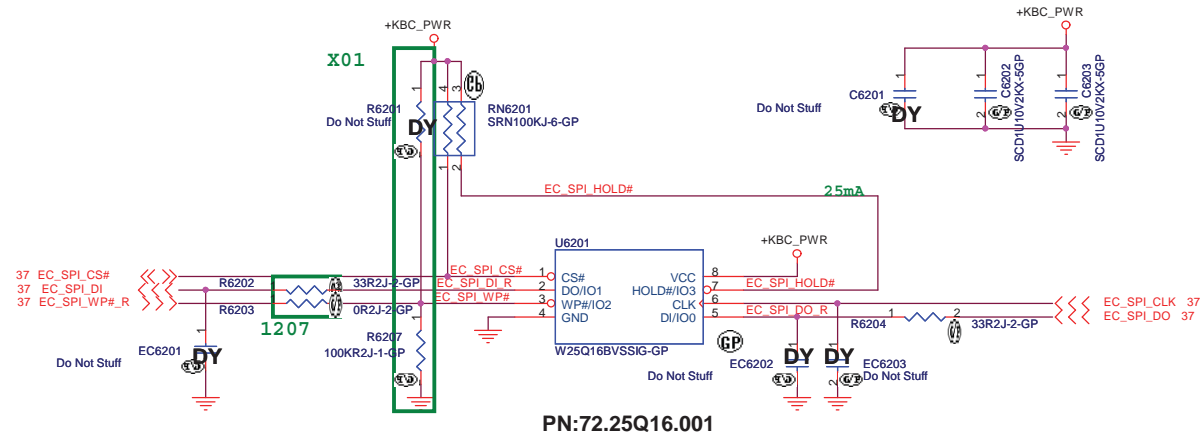
3 DJ2 AMD UMA (10 100 w HDMI)

DELL Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

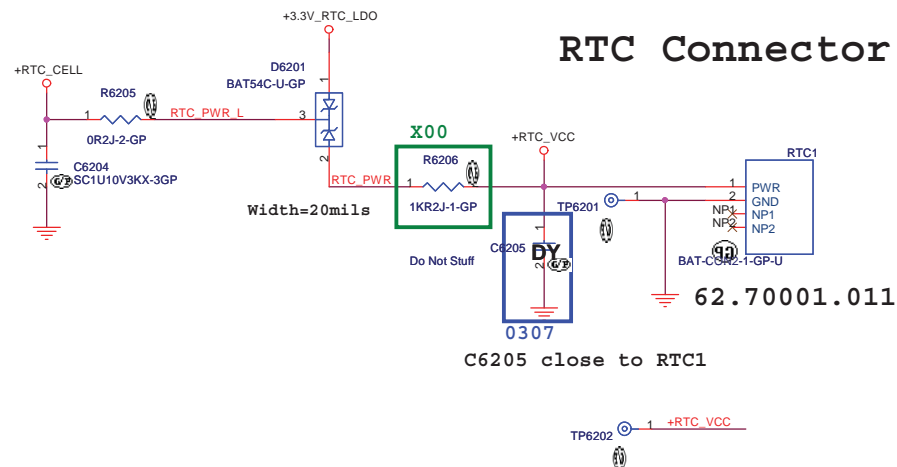
Title		XFORM/RJ45	
Size	Document Number	Rev	
A3	Chelsea DJ2 AMD UMA	X01	
Date:	Tuesday, April 13, 2010	Sheet	61 of 90

SSID = Flash.ROM

SPI FLASH ROM (16M bits) for KBC



SSID = RBATT



3 DJ2 AMD UMA (10 100 w HDMI)

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

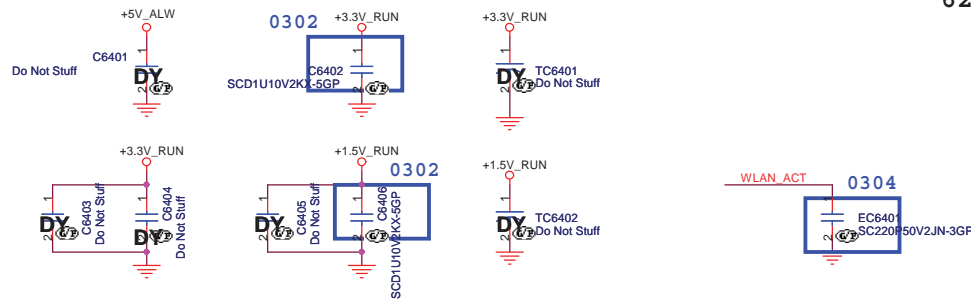
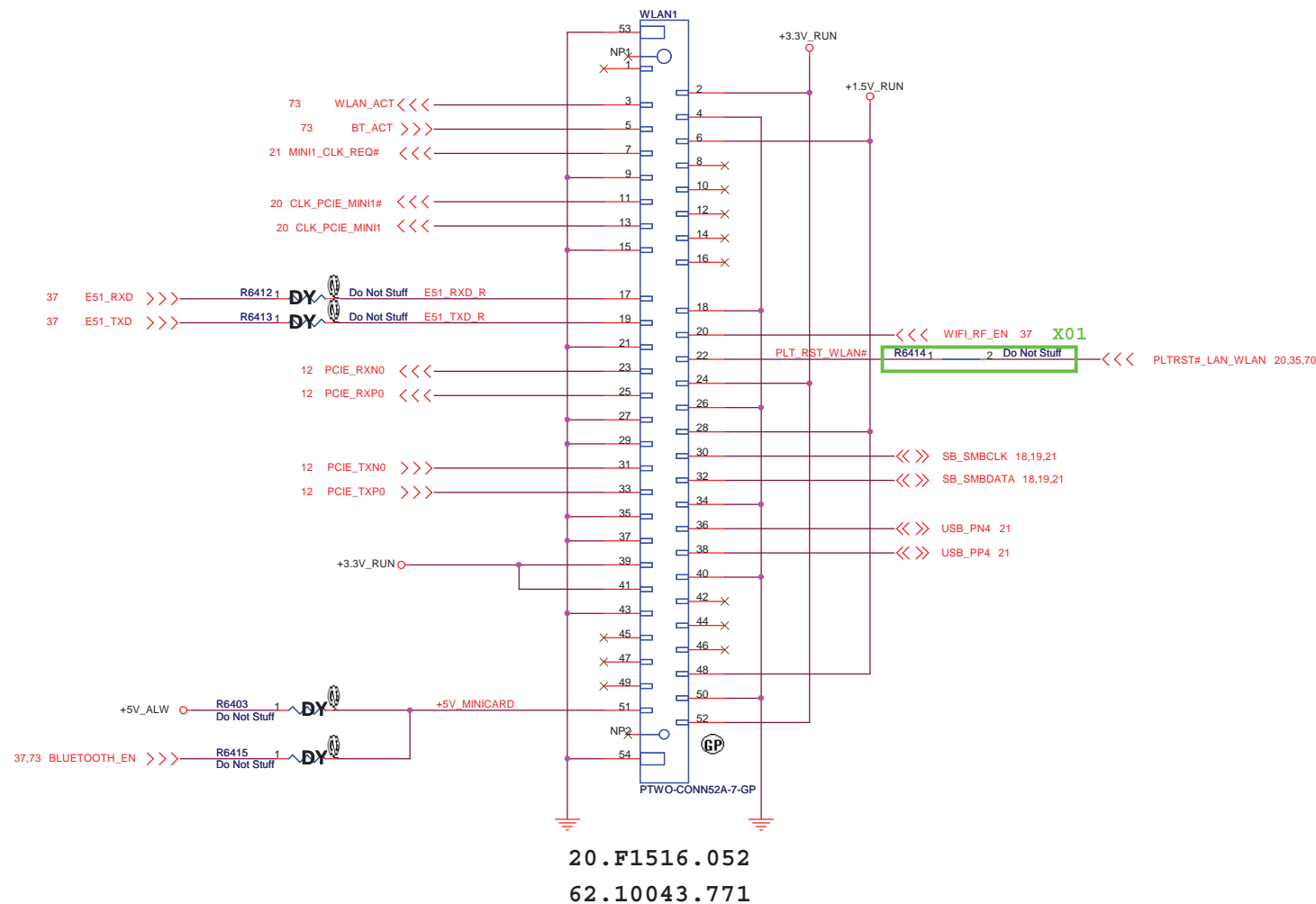
Title			Flash/RTC	
Size	Document Number	Rev		
A3	Chelsea DJ2 AMD UMA	X01		
Date:	Tuesday, April 13, 2010	Sheet	62	of 90

0222



SSID = Wireless

Mini Card Connector(802.11a/b/g)



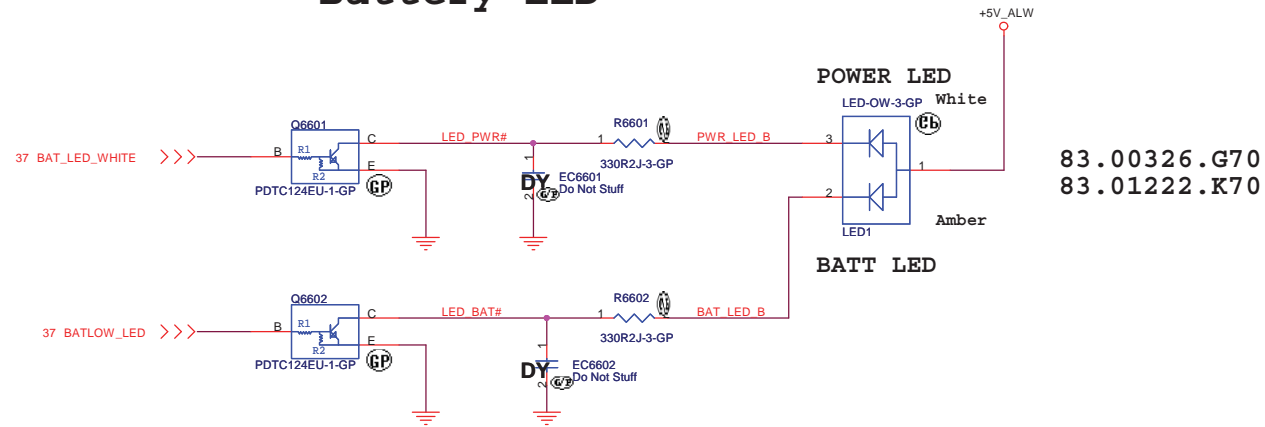
3 DJ2 AMD UMA (10 100 w HDMI)

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

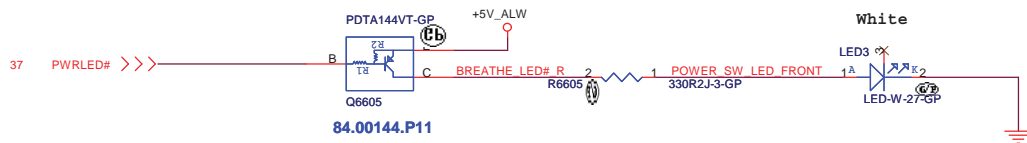
Title		MINICARD	
Size	Document Number	Rev	X01
A3	Chelsea DJ2 AMD UMA		
Date:	Tuesday, April 13, 2010	Sheet	64 of 90

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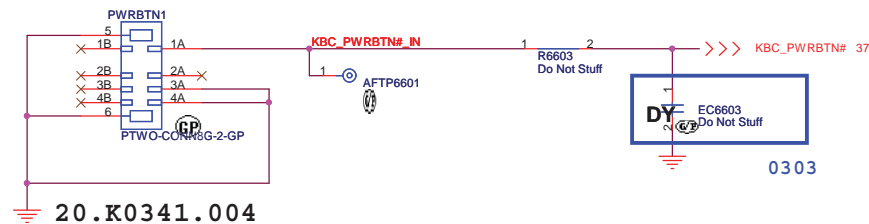
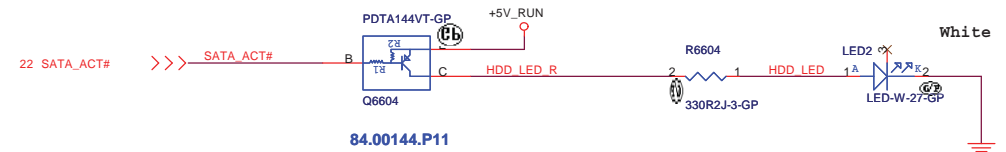
Battery LED



BREATHE PWR LED (Front)



HDD LED

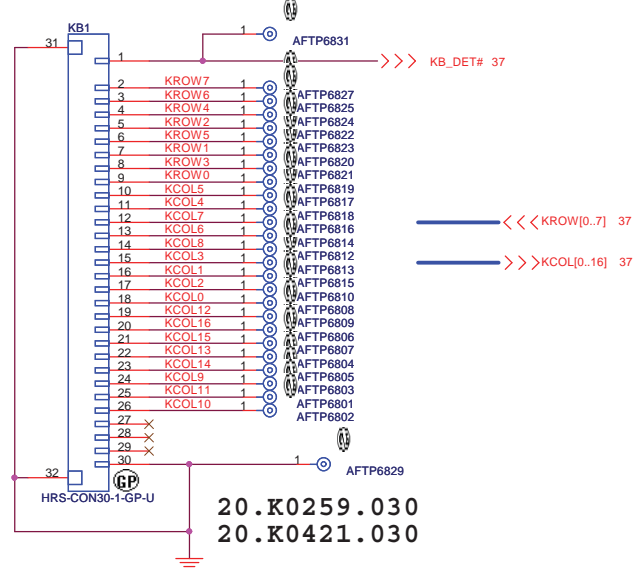


3 DJ2 AMD UMA (10 100 w HDMI)

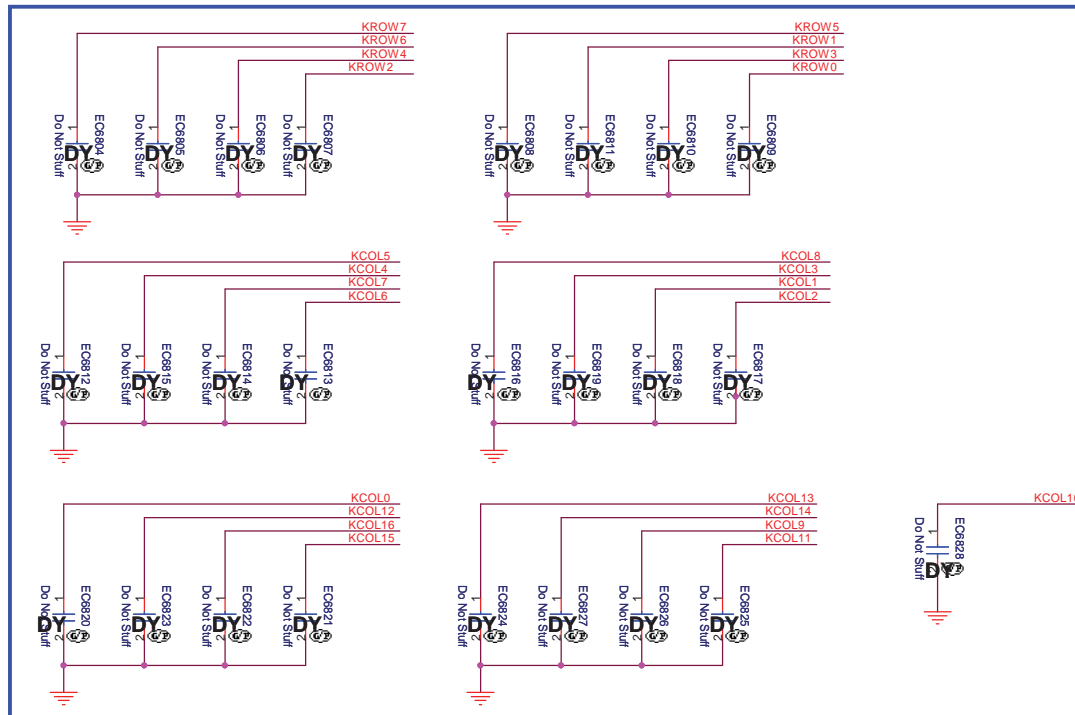
DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			LED/PWRBTN	
Size	Document Number	Rev		
A3	Chelsea DJ2 AMD UMA	X01		
Date:	Tuesday, April 13, 2010	Sheet	66	of 90

Internal Keyboard Connector

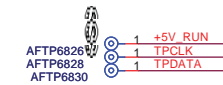
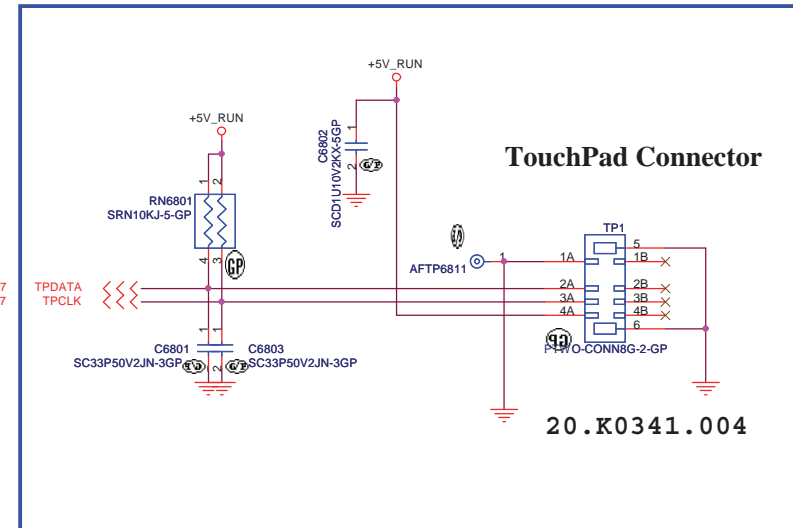


0304



SSID = Touch.Pad

0302

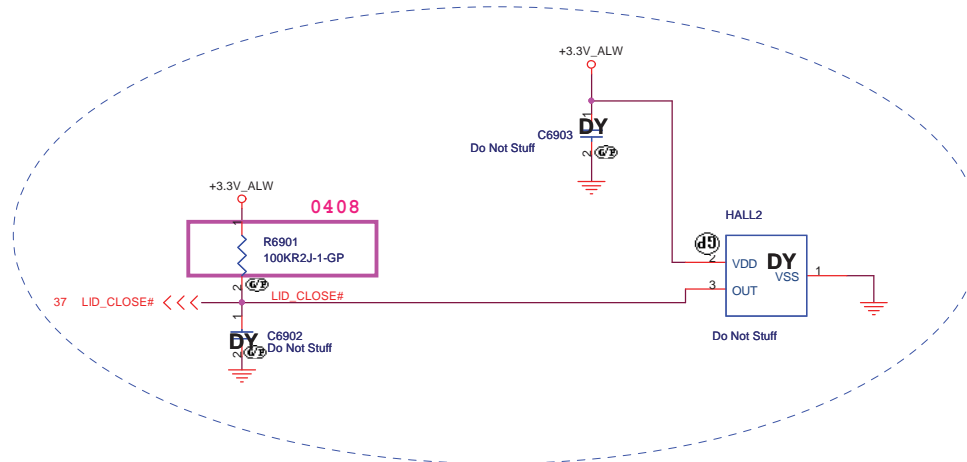
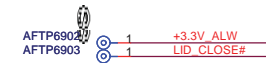
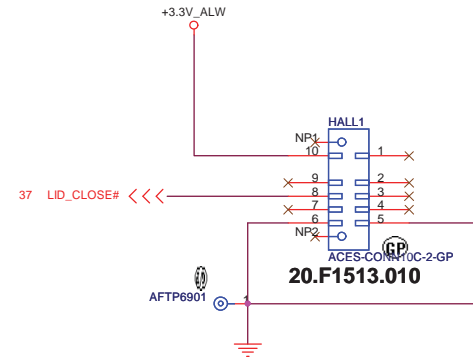


3 DJ2 AMD UMA (10 100 w HDMI)

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
Key Board/Touch Pad		
Size A3	Document Number	Rev
	Chelsea DJ2 AMD UMA	X01
Date: Tuesday, April 13, 2010	Sheet 68	of 90

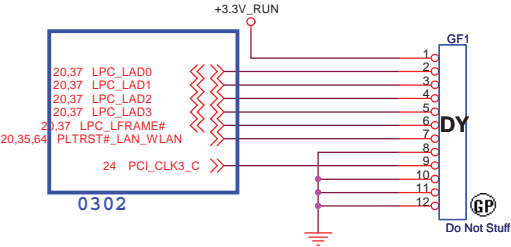
SSID = User. Interface



3 DJ2 AMD UMA (10 100 w HDMI)

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			Hall Sensor		
Size	Document Number	Rev			
A3	Chelsea DJ2 AMD UMA	X01			
Date:	Tuesday, April 13, 2010	Sheet	69	of	90

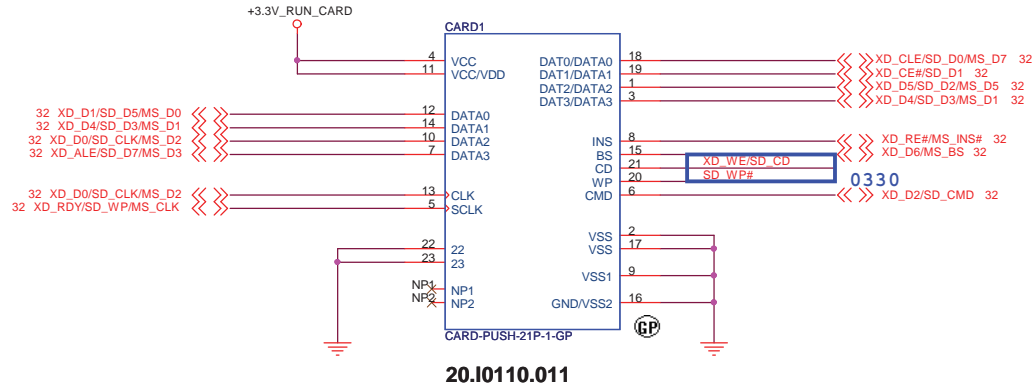
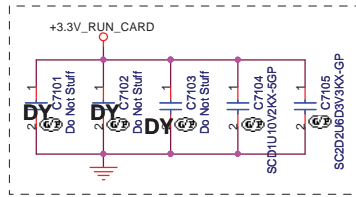


3 DJ2 AMD UMA (10 100 w HDMI)

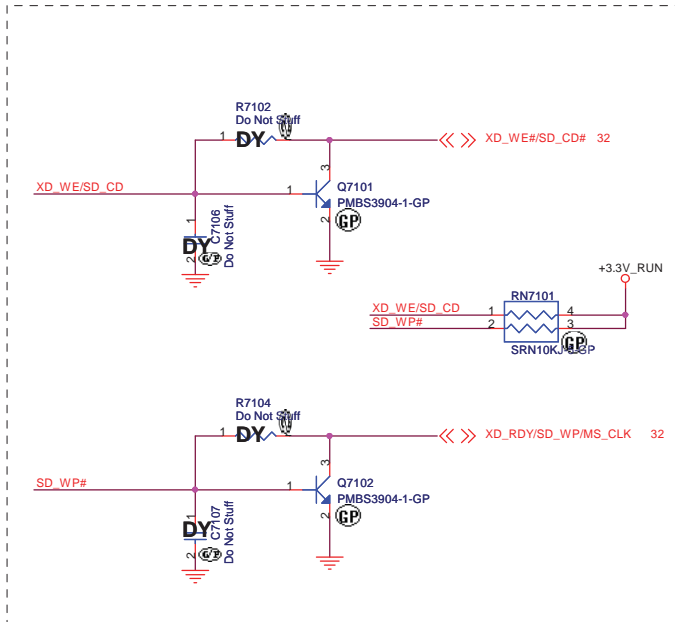
DELL		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
Size A3	Document Number Chelsea DJ2 AMD UMA	Rev X01	
Date: Tuesday, April 13, 2010	Sheet 70 of 90		

SD/XD/MS Card Reader

SSID = SDIO



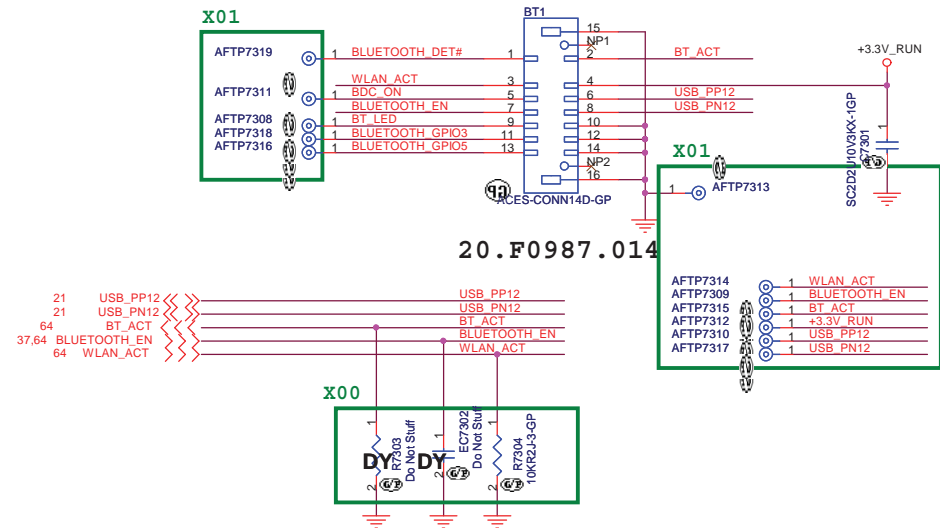
For reverse card connector 0330



3 DJ2 AMD UMA (10 100 w HDMI)

SSID = User.Interface

Bluetooth Module conn.



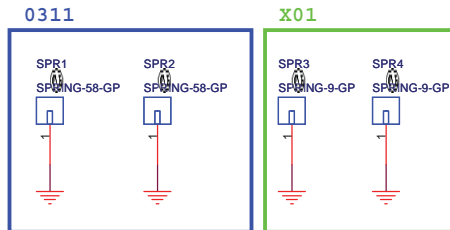
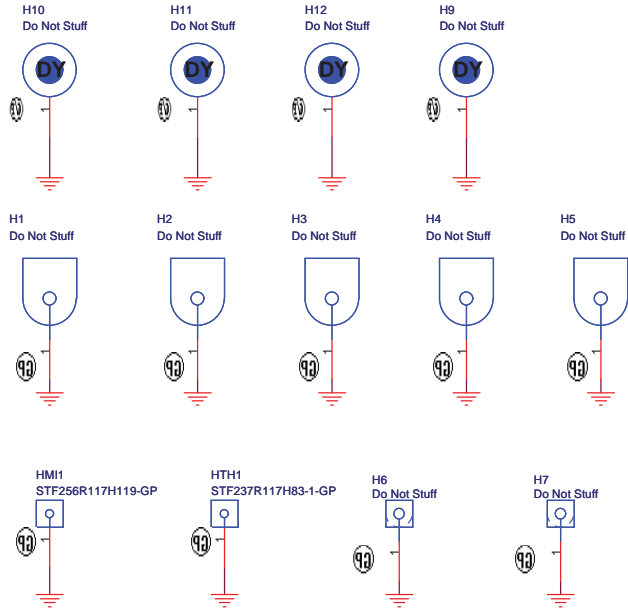
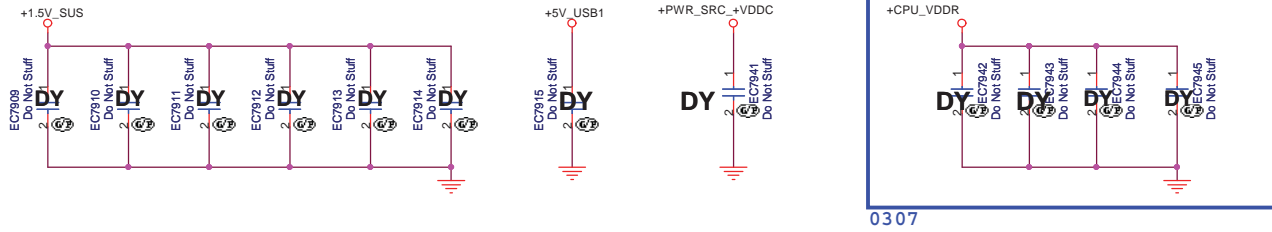
3 DJ2 AMD UMA (10 100 w HDMI)



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